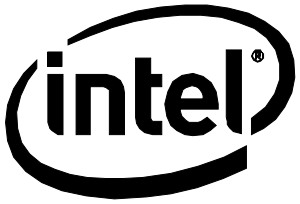


Intel® Desktop Board DP67BG

Technical Product Specification

December 2012

Order Number: G13848-002

The Intel® Desktop Board DP67BG may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board DP67BG Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board DP67BG Technical Product Specification	January 2011
-002	Specification Clarification	December 2012

This product specification applies to only the standard Intel® Desktop Board DP67BG with BIOS identifier BGP6710J.86A.

Changes to this specification will be published in the Intel Desktop Board DP67BG Specification Update before being incorporated into a revision of this document.

Board Identification Information

Basic Desktop Board DP67BG Identification Information

AA Revision	BIOS Revision	Notes
G10491-200	BGP6710J.86A.1220	1,2
G10491-303	BGP6710J.86A.1900	1,2
G10491-304	BGP6710J.86A.1900	1,2

Notes:

1. The AA number is found on a small label on the component side of the board.
2. The P67 chipset used on this AA revision consists of the following component:

Device	Stepping	S-Spec Numbers
82P67	B2	SLH84
82P67	B3	SLJ4C

Specification Changes or Clarifications

The table below indicates the Specification Changes or Specification Clarifications that apply to the Intel® Desktop Board DP67BG.

Specification Changes or Clarifications

Date	Type of Change	Description of Change or Clarification
December 2012	Spec Clarification	Updated Table 27. Environmental Specifications to address operating temperature requirements for the board.

Errata

Current characterized errata, if any, are documented in a separate Specification Update. See http://developer.intel.com/products/desktop/motherboard/index.htm for the latest documentation.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel® Desktop Board DP67BG.

Intended Audience

The TPS is intended to provide detailed, technical information about the Intel Desktop Board DP67BG and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the Intel Desktop Board DP67BG
2	A map of the resources of the Intel Desktop Board
3	The features supported by the BIOS Setup program
4	A description of the BIOS error messages, beep codes, and POST codes
5	Regulatory compliance and battery disposal information

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
GB	Gigabyte (1,073,741,824 bytes)
GB/s	Gigabytes per second
Gb/s	Gigabits per second
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/s	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/s	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbits/s	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

Figures

Tables

1 Product Description

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the major features of the board.

Table 1. Feature Summary

Form Factor	ATX (12.00 inches by 9.60 inches [304.80 millimeters by 243.84 millimeters])
Processor	• Intel® Core™ i7, Intel® Core™ i5, and Intel® Core™ i3 processors with up to 95 W TDP in an LGA1155 socket: — 1 x16 PCIe 2.0 Graphics interface (operates in x8 mode when second slot is populated) — Two DDR3 memory channels
Memory	• Four 240-pin DDR3 SDRAM Dual Inline Memory Module (DIMM) sockets • Support for DDR3 +1600 MHz, DDR3 1333 MHz, and DDR3 1066 MHz DIMMs • Support for 1 Gb, 2 Gb, and 4 Gb memory technology • Support for up to 32 GB of system memory with four DIMMs using 4 Gb memory technology • Support for non-ECC memory • Support for 1.35 V low voltage JEDEC memory • Support for XMP memory
Chipset	Intel® P67 Express Chipset consisting of the Intel® P67 Platform Controller Hub (PCH)
Audio	Intel® High Definition Audio subsystem using the Realtek* ALC892 audio codec
Legacy I/O Control	Nuvoton* legacy I/O controller for Consumer Infrared (CIR)
Peripheral Interfaces	• Two USB 3.0 ports are implemented with stacked back panel connectors (blue) • Fourteen USB 2.0 ports: — Eight ports are implemented with stacked back panel connectors (black) — Six front panel ports implemented through three internal headers • Two Serial ATA (SATA) 6.0 Gb/s interfaces through the Intel P67 Express Chipset with Intel® Rapid Storage Technology RAID support (blue) • Four internal SATA 3.0 Gb/s interfaces through the Intel P67 Express Chipset with Intel Rapid Storage Technology RAID support (black) • One back panel eSATA port (red) • Two IEEE 1394a ports: — One port via a back panel connector — One port via a front-panel header (blue)
Wireless Module	• Separate module that provides both Bluetooth* and WiFi included with the desktop board (optional)
BIOS	• Intel® BIOS resident in the SPI Flash device • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS

continued

Table 1. Feature Summary (continued)

Instantly Available PC Technology	• Support for PCI* Local Bus Specification Revision 2.2 • Support for PCI Express* Revision 2.0 • Suspend to RAM support • Wake on PCI, PCI Express, LAN, front panel, CIR, and USB ports
LAN Support	Gigabit (10/100/1000 Mbits/s) LAN subsystem using the Intel® 82579V Gigabit Ethernet Controller
Expansion Capabilities	• Two PCI Express 2.0 x16 • Three PCI Express x1 bus add-in card connectors from the PCH • Two Conventional PCI bus add-in card connectors from the PCH via PCI bridge
Hardware Monitor Subsystem	• Hardware monitoring and fan control through the Nuvoton I/O controller • Voltage sense to detect out of range power supply voltages • Thermal sense to detect out of range thermal values • Four fan headers using PWM control • Four fan sense inputs used to monitor fan activity • Fan speed control using voltage control (4-pin fan headers front, rear, and auxiliary) with selectable support in BIOS for 3 wire fans • Support for Platform Environmental Control Interface (PECI)

1.1.2 Board Layout

Figure 1 shows the location of the major components on Intel Desktop Board DP67BG.

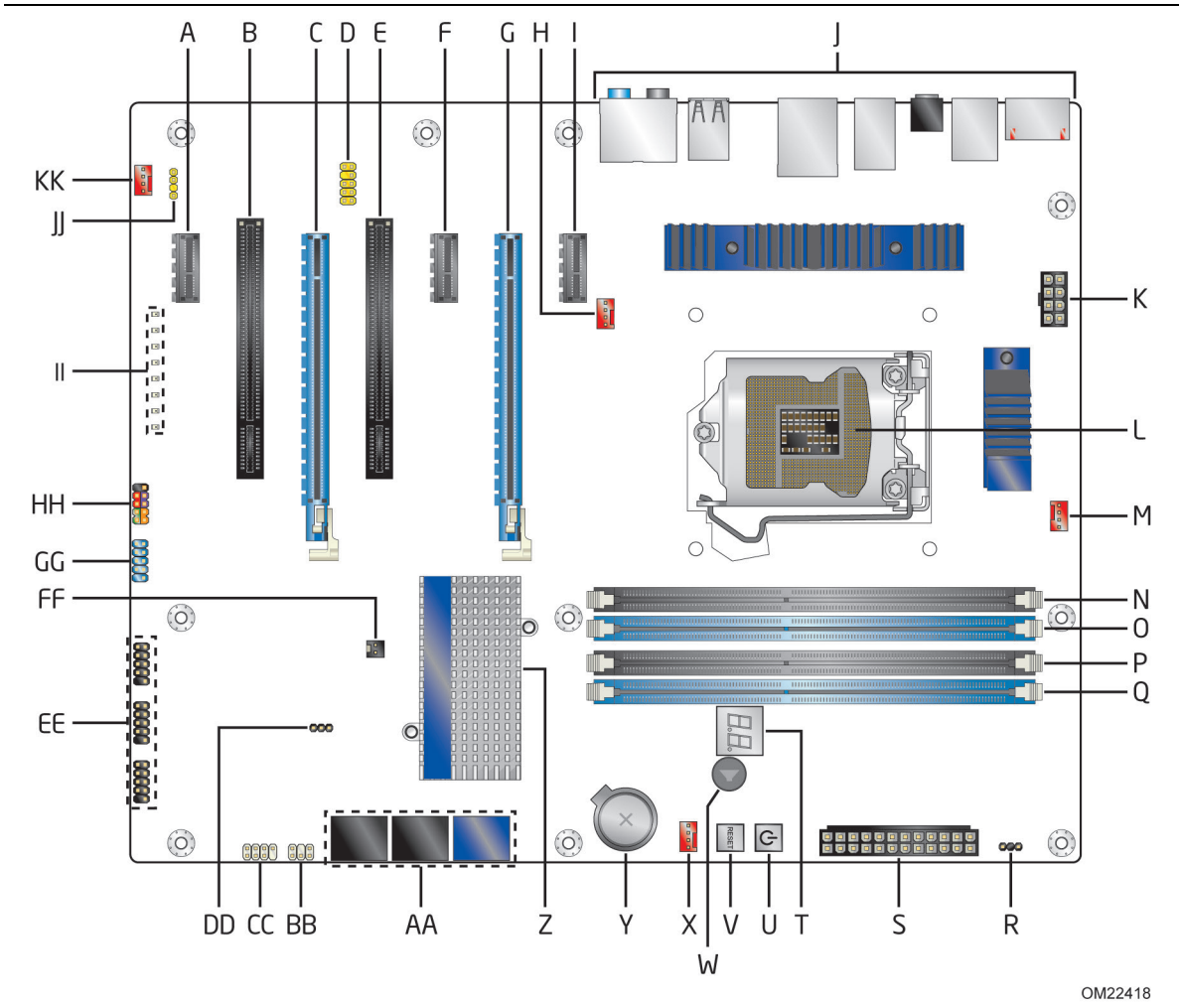


Figure 1. Major Board Components

Table 2 lists the components identified in Figure 1.

Table 2. Components Shown in Figure 1

Label	Description
A	PCI Express x1 bus add-in card connector
B	Conventional PCI bus add-in card connector
C	PCI Express 2.0 x16 connector (x8 electrical; x16 compatible)
D	Front panel audio header
E	Conventional PCI bus add-in card connector
F	PCI Express x1 bus add-in card connector
G	PCI Express 2.0 x16 bus add-in card connector
H	Rear chassis fan header
I	PCI Express x1 bus add-in card connector
J	Back panel connectors
K	12 V processor core voltage connector (2 x 4 pin)
L	LGA1155 processor socket
M	Processor fan header
N	DIMM 3 (Channel A DIMM 0)
O	DIMM 1 (Channel A DIMM 1)
P	DIMM 4 (Channel B DIMM 0)
Q	DIMM 2 (Channel B DIMM 1)
R	Alternate front panel power LED header
S	Main power connector (2 x 12 pin)
T	POST code LED display
U	Onboard power button
V	Onboard reset button
W	Speaker
X	Front chassis fan header
Y	Battery
Z	Intel P67 Express Chipset
AA	SATA connectors (6)
BB	Consumer IR transmitter (output) header
CC	Consumer IR receiver (input) header
DD	BIOS Setup configuration jumper block
EE	Front panel USB 2.0 headers (3)
FF	Chassis intrusion header
GG	IEEE 1394a front panel header
HH	Front panel header
II	Diagnostic LEDs
JJ	S/PDIF out header
KK	Auxiliary fan header

1.1.3 Block Diagram

Figure 2 is a block diagram of the major functional areas of the board.

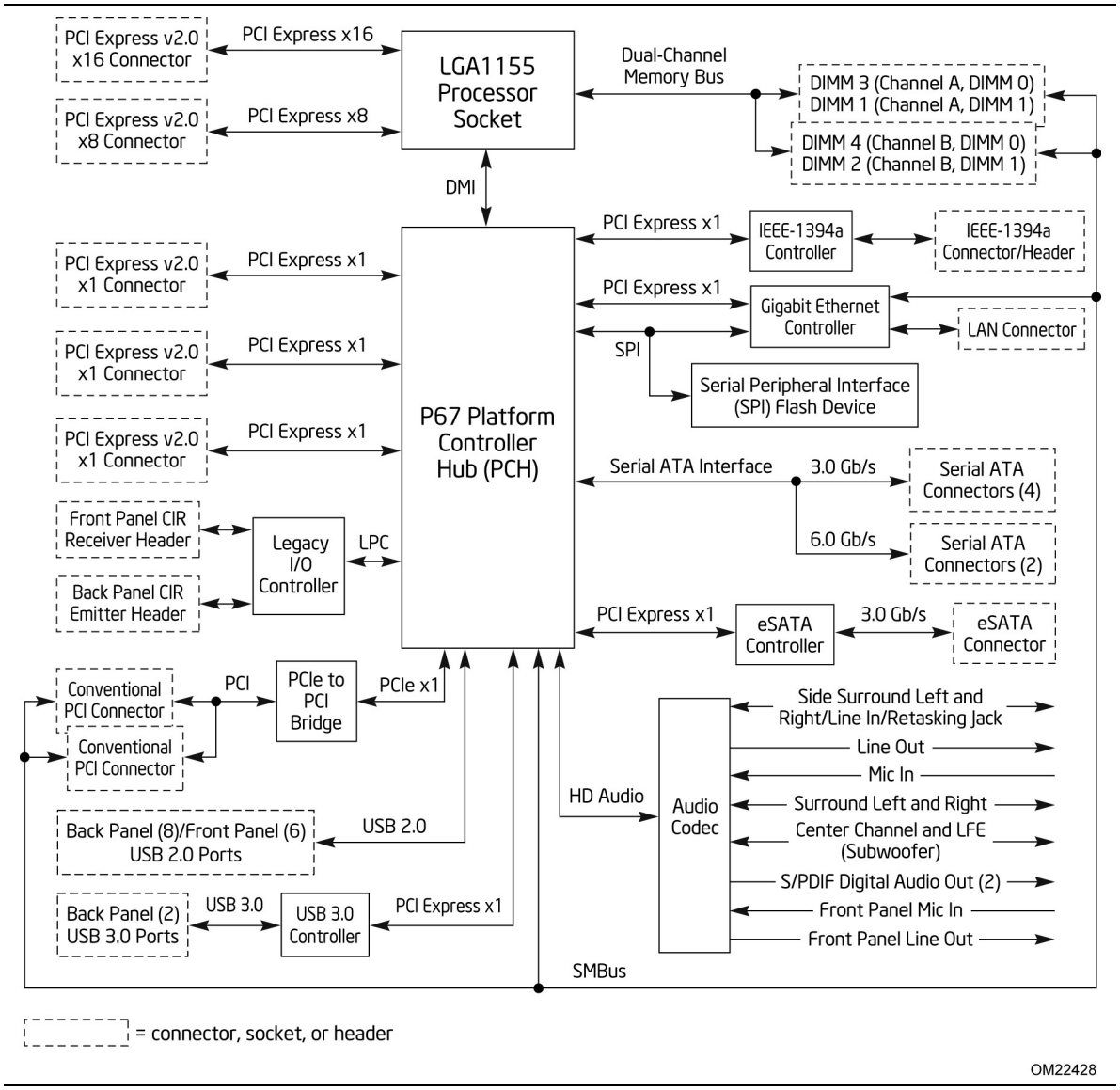


Figure 2. Block Diagram

1.2 Legacy Considerations

This board differs from other Intel Desktop Board products, with specific changes including (but not limited to) the following:

- No parallel port connector
- No floppy drive connector
- No PS/2 connectors

1.3 Online Support

To find information about…	Visit this World Wide Web site:
Intel Desktop Board DP67BG	http://www.intel.com/products/motherboard/index.htm
Desktop Board Support	http://www.intel.com/p/en_US/support?iid=hdr+support
Available configurations for the Intel Desktop Board DP67BG	http://ark.intel.com
Supported processors	http://processormatch.intel.com
Chipset information	http://www.intel.com/products/desktop/chipsets/index.htm
BIOS and driver updates	http://downloadcenter.intel.com
Tested memory	http://www.intel.com/support/motherboards/desktop/sb/CS-025414.htm
Integration information	http://www.intel.com/support/go/buildit

1.4 Processor

The board is designed to support the Intel Core i7, Intel Core i5, and Intel Core i3 processors in an LGA1155 socket

Other processors may be supported in the future. This board is designed to support processors with a maximum wattage of 95 W with margin to allow for greater than 150 W operation. The processors listed above are only supported when falling within the wattage requirements of the Intel Desktop Board DP67BG. See the Intel web site listed below for the most up-to-date list of supported processors.

For information about…	Refer to:
Supported processors	http://processormatch.intel.com

CAUTION

Use only the processors listed on the web site above. Use of unsupported processors can damage the board, the processor, and the power supply.

NOTE

This board has specific requirements for providing power to the processor. Refer to Section 2.5.1 on page 57 for information on power supply requirements for this board.

1.4.1 PCI Express x16 Graphics

The Intel Core i7, Intel Core i5, and Intel Core i3 processors in an LGA1155 socket support discrete add in graphics cards via the PCI Express 2.0 x16 graphics connector:

- Supports PCI Express GEN2 frequency of 2.5 GHz resulting in 5.0 Gb/s each direction (500 MB/s) per lane. The maximum theoretical bandwidth on the interface is 8 GB/s in each direction, simultaneously, for an aggregate of 16 GB/s when operating in x16 GEN2 mode.
- Supports PCI Express GEN1 frequency of 1.25 GHz resulting in 2.5 Gb/s each direction (250 MB/s) per lane. The maximum theoretical bandwidth on the interface is 4 GB/s in each direction, simultaneously, for an aggregate of 8 GB/s when operating in x16 GEN1 mode.

For information about	Refer to
PCI Express technology	http://www.pcisig.com

1.5 System Memory

The board has four DIMM sockets and supports the following memory features:

- 1.35 V DDR3 SDRAM DIMMs (New JEDEC Specification)
- Two independent memory channels with interleaved mode support
- Unbuffered, single-sided or double-sided DIMMs with the following restriction:
  Double-sided DIMMs with x16 organization are not supported.
- 32 GB maximum total system memory (using 4 Gb memory technology). Refer to Section 2.1.1 on page 41 for information on the total amount of addressable memory.
- Minimum total system memory: 1 GB using 512 MB x16 module
- Non-ECC DIMMs
- Serial Presence Detect
- DDR3 +1600 MHz, 1333 MHz, and DDR3 1066 MHz SDRAM DIMMs
- XMP version 1.2 performance profile support for memory speeds above 1600 MHz

NOTE

To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.

Table 3 lists the supported DIMM configurations.

Table 3. Supported Memory Configurations

DIMM Capacity	Configuration (Note)	SDRAM Density	SDRAM Organization Front-side/Back-side	Number of SDRAM Devices
512 MB	SS	1 Gbit	64 M x16/empty	4
1024 MB	SS	1 Gbit	128 M x8/empty	8
1024 MB	SS	2 Gbit	128 M x16/empty	4
2048 MB	DS	1 Gbit	128 M x8/128 M x8	16
2048 MB	SS	2 Gbit	128 M x16/empty	8
4096 MB	DS	2 Gbit	256 M x8/256 M x8	16
4096 MB	SS	4 Gbit	512 M x8/empty	8
8192 MB	DS	4 Gbit	512 M x8/512 M x8	16

Note: "DS" refers to double-sided memory modules (containing two rows of SDRAM) and "SS" refers to single-sided memory modules (containing one row of SDRAM).

For information about...	Refer to:
Tested Memory	http://support.intel.com/support/motherboards/desktop/sb/CS-025414.htm
XMP Tested Memory	http://www.intel.com/personal/gaming/extrememory.htm

1.5.1 Memory Configurations

The Intel Core i7, Intel Core i5, and Intel Core i3 processors support the following types of memory organization:

- **Dual channel (Interleaved) mode**. This mode offers the highest throughput for real world applications. Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speed DIMMs are used between channels, the slowest memory timing will be used.
- **Single channel (Asymmetric) mode**. This mode is equivalent to single channel bandwidth operation for real world applications. This mode is used when only a single DIMM is installed or the memory capacities are unequal. Technology and device width can vary from one channel to the other. If different speed DIMMs are used between channels, the slowest memory timing will be used.

For information about…	Refer to:
Memory Configuration Examples	http://www.intel.com/support/motherboards/desktop/sb/cs-011965.htm

Figure 3 illustrates the memory channel and DIMM configuration.

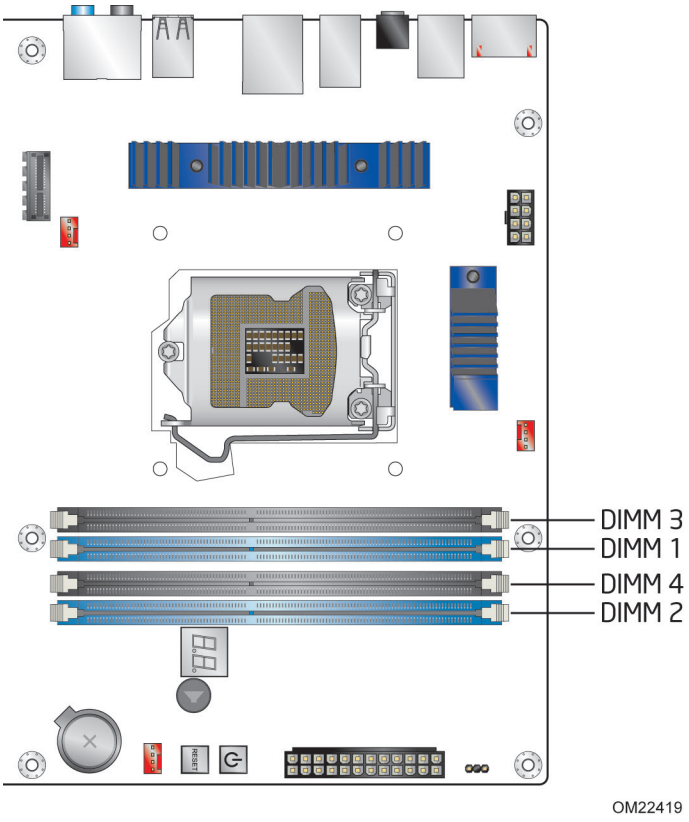


Figure 3. Memory Channel and DIMM Configuration

NOTE

The Intel Core i7, Intel Core i5, and Intel Core i3 processors require memory to be populated in the DIMM 1 (Channel A, DIMM 0) socket.

For best memory performance always install memory into the blue DIMM memory sockets if only installing two DIMMs in your configuration.

1.6 Intel® P67 Express Chipset

The Intel P67 Express Chipset consisting of the Intel P67 Platform Controller Hub (PCH) provides interfaces to the processor and the USB, SATA, LAN, PCI, and PCIe interfaces. The PCH is a centralized controller for the board's I/O paths.

For information about	Refer to
The Intel P67 Express Chipset	http://www.intel.com/products/desktop/chipsets/index.htm
Resources used by the chipset	Chapter 2

1.6.1 USB

The board supports up to 14 USB 2.0 ports and two USB 3.0 ports.

The Intel P67 Express Chipset provides the USB controller for the 2.0 ports. The two USB 3.0 ports are provided by the NEC* UPD720200 controller. The port arrangement is as follows:

- Two USB 3.0 ports are implemented with stacked back panel connectors (blue)
- Eight USB 2.0 ports are implemented with stacked back panel connectors (black)
- Six USB 2.0 front panel ports implemented through four internal headers

All 16 USB ports are high-speed, full-speed, and low-speed capable. The USB 3.0 ports are super-speed capable.

NOTES

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use a shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 10, page 44
The location of the front panel USB headers	Figure 11, page 45

1.6.2 SATA Interfaces

The board provides six SATA connectors through the PCH and one eSATA connector through a Marvell controller, which support one device per connector:

- Two internal SATA 6.0 Gb/s connectors (blue)
- Four internal SATA 3.0 Gb/s connectors (black)
- One eSATA 3.0 Gb/s connector on the back panel for external connectivity (red)

The PCH provides independent SATA ports with a theoretical maximum transfer rate of 6 Gb/s for two ports and 3 Gb/s for five ports. A point-to-point interface is used for host to device connections.

The underlying SATA functionality is transparent to the operating system. The SATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for

configurations using the Windows* XP, Windows Vista*, and Windows 7* operating systems.

NOTE

Many SATA drives use new low-voltage power connectors and require adapters or power supplies equipped with low-voltage power connectors.

For more information, see: http://www.serialata.org/.

For information about	Refer to
The location of the SATA connectors	Figure 11, page 45

1.6.2.1 SATA RAID

The board supports the following RAID (Redundant Array of Independent Drives) levels via the PCH:

- **RAID 0** - data striping
- **RAID 1** - data mirroring
- **RAID 0+1 (or RAID 10)** - data striping and mirroring
- **RAID 5** - distributed parity

RAID functionality is only supported when using drives connected to the six SATA connectors (black) from the PCH.

NOTE

In order to use supported RAID features, you must first enable RAID in the BIOS. Also, during Microsoft Windows XP installation, you must press F6 to install the RAID drivers. See your Microsoft Windows XP documentation for more information about installing drivers during installation. Both Microsoft Windows Vista and Microsoft Windows 7 include the necessary RAID drivers for both AHCI and RAID without the need to install separate RAID drivers using the F6 switch in the operating system installation process.

1.7 Real-Time Clock Subsystem

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied via the power supply 5V STBY rail.

NOTE

If the battery and AC power fail date and time values will be reset and the user will be notified during POST.

When the voltage drops below a certain level, the BIOS Setup program settings stored in CMOS RAM (for example, the date and time) might not be accurate. Replace the battery with an equivalent one. Figure 1 on page 13 shows the location of the battery.

1.8 Legacy I/O Controller

The I/O controller provides the following features:

- Consumer Infrared (CIR) headers
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support

The BIOS Setup program provides configuration options for the I/O controller.

1.8.1 Consumer Infrared (CIR)

The Consumer Infrared (CIR) feature is designed to comply with Microsoft Consumer Infrared usage models. Microsoft Windows Vista and Microsoft Windows 7 are the supported operating systems.

The CIR feature is made up of two separate pieces: the receiving (receiver) header, and the output (emitter) header. The receiving header consists of a filtered translated infrared input compliant with Microsoft CIR specifications, and also a "learning" infrared input. This learning input is simply a high pass input which the computer can use to "learn" to speak the infrared communication language of other user remotes. The emitter header consists of two output ports which the PC can use to emulate "learned" infrared commands in order to control external electronic hardware.

Customers are required to buy or create their own interface modules to plug into Intel Desktop Boards for this feature to work.

1.9 Audio Subsystem

The board supports the Intel High Definition Audio subsystem based on the Realtek ALC892 audio codec. The audio subsystem supports the following features:

- Advanced jack sense for the back panel audio jacks that enables the audio codec to recognize the device that is connected to an audio port. The back panel audio jacks are capable of retasking according to the user's definition, or can be automatically switched depending on the recognized device type.
- Stereo input and output for all back panel jacks
- Line out and Mic in functions for front panel audio jacks
- A signal-to-noise (S/N) ratio of 90 dB

Table 4 lists the supported functions of the front panel and back panel audio jacks.

Table 4. Audio Jack Support

Audio Jack	Micro-phone	Head-phones	Front Speaker	Line In	Rear Surround	Center/ Sub	Side Surround
FP Green		Default					
FP Pink	Default						
Rear Blue				Default			
Rear Green		Ctrl panel	Default				
Rear Pink	Default						Ctrl panel
Rear Black					Default		
Rear Orange						Default	

1.9.1 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

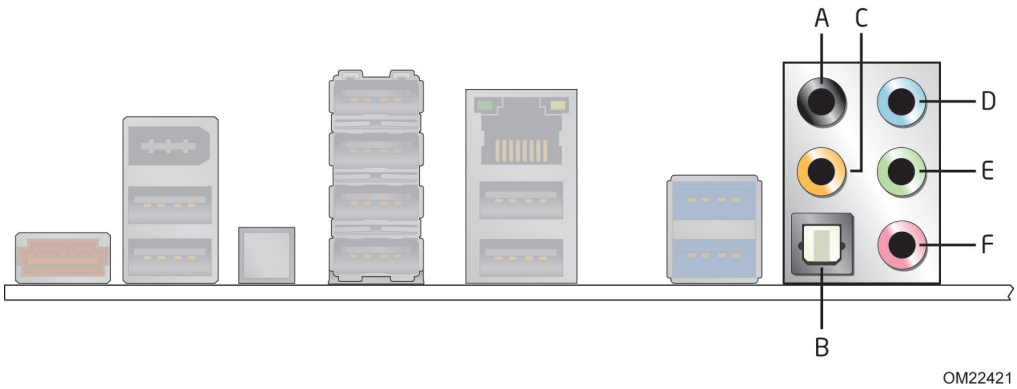
For information about	Refer to
Obtaining audio software and drivers	Section 1.3, page 16

1.9.2 Audio Subsystem Components

The audio subsystem includes the following components:

- Intel P67 Express Chipset
- Realtek ALC892 audio codec
- Front panel audio header that supports Intel HD audio and AC '97 audio (a 2 x 5-pin header that provides mic in and line out signals for front panel audio connectors) (yellow)
- S/PDIF digital audio out header (1 x 4-pin header) (yellow)
- S/PDIF digital audio out connector on the back panel
- 5-port analog audio input/output stack on the back panel

The back panel audio connectors are configurable through the audio device drivers. The available configurable back panel audio connectors are shown in Figure 4.



Item	Description
A	Rear surround
B	S/PDIF out (optical)
C	Center channel and LFE (Subwoofer)
D	Line in
E	Line out/front speakers
F	Mic in/side surround

Figure 4. Back Panel Audio Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

For information about	Refer to
The locations of the front panel audio header and S/PDIF audio header	Figure 11, page 45
The signal names of the front panel audio header and S/PDIF audio header	Section 2.2.2.1, page 47
The back panel audio connectors	Section 2.2.1, page 44

1.10 LAN Subsystem

The LAN subsystem consists of the following:

- Intel 82579V Gigabit Ethernet Controller (10/100/1000 Mbits/s)
- Intel P67 Express Chipset
- RJ-45 LAN connector with integrated status LEDs

Additional features of the LAN subsystem include:

- CSMA/CD protocol engine
- LAN connect interface between the PCH and the LAN controller
- Conventional PCI bus power management
  - ACPI technology support
  - LAN wake capabilities
- LAN subsystem software

For information about	Refer to
LAN software and drivers	http://downloadcenter.intel.com

1.10.1 Intel® 82579V Gigabit Ethernet Controller

The Intel 82579V Gigabit Ethernet Controller supports the following features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Energy Efficient Ethernet (EEE) IEEE802.3az support [Low Power Idle (LPI) mode]
- Dual interconnect between the Integrated LAN Controller and the Physical Layer (PHY):
  - PCI Express-based interface for active state operation (S0) state
  - SMBUS for host and management traffic (Sx low power state)
- Compliant to IEEE 802.3x flow control support
- 802.1p and 802.1q
- TCP, IP, and UDP checksum offload (for IPv4 and IPv6)
- Full device driver compatibility
- Provides lower power usage to meet Energy Star 5.0 and ErP specifications

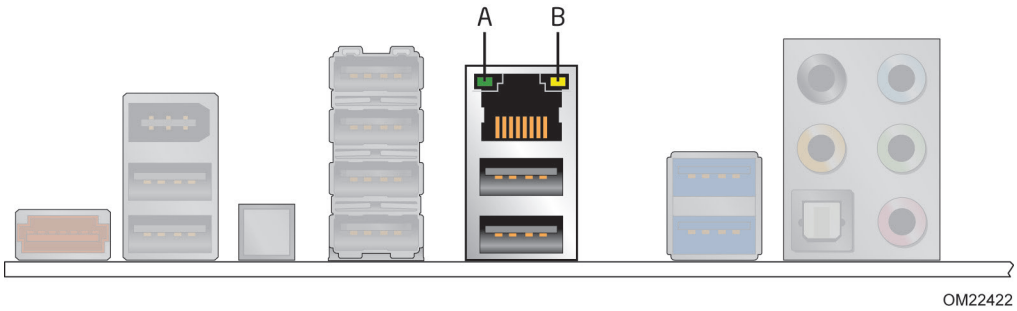
1.10.2 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	http://downloadcenter.intel.com

1.10.3 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 5).



Item	Description
A	Link LED (green)
B	Data Rate LED (green/yellow)

Figure 5. LAN Connector LED Locations

Table 5 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 5. LAN Connector LED States

LED	LED Color	LED State	Condition
Link	Green	Off	LAN link is not established.
		On	LAN link is established.
		Blinking	LAN activity is occurring.
Data Rate	Green/Yellow	Off	10 Mbits/s data rate is selected.
		Green	100 Mbits/s data rate is selected.
		Yellow	1000 Mbits/s data rate is selected.

1.11 Bluetooth*/WiFi Module (optional)

The WiFi/Bluetooth*module is supplemental hardware that is included with certain Desktop Boards.

1.11.1 Bluetooth Technology (Module)

The Bluetooth Module enables the user to connect with a variety of Bluetooth enabled devices. Driver support is provided by Microsoft operating systems like Microsoft Vista and Microsoft Windows 7. The Bluetooth driver stack is supplied by Microsoft but some Bluetooth enable devices might provide additional Bluetooth features and for proper functioning of those features, will need their own supplied drivers installed.

- CSR Bluetooth module (BC0401PC08)
- Maximum data rate 3.0Mb/s
- Forward and backward compatibility with Bluetooth v1.1, v1.2, v2.0 and v2.1
- Integrated Antenna
- Operating system support (Windows XP, Vista and 7 both 32 bit and 64 bit)

For information about	Refer to
Obtaining Bluetooth information and drivers	http://msdn.microsoft.com/en-us/library/aa362932(VS.85).aspx

1.11.2 WiFi 802.11 Wireless (Module)

The WiFi Module enables the user to connect with a variety of WiFi enabled networks, access points and allows peer to peer connections. Driver support is provided by Microsoft operating systems like Microsoft Vista and Microsoft Windows 7 with additional support provided by the supplied WiFi driver included on the Driver DVD and online.

- Ralink WiFi 802.11 (RT8070)
- Range up to 300 meters
- Supports the following:
  - IEEE 802.11B supports up to 11 Mb/s data rate
  - IEEE 802.11G supports up to 54 Mb/s data rate
  - IEEE 802.11N supports up to 150 Mb/s data rate
- Integrated Antenna
- Operating system support (Windows XP, Vista and 7 both 32 bit and 64 bit)

For information about	Refer to
Obtaining WiFi information and drivers	http://msdn.microsoft.com/en-us/library/aa362932(VS.85).aspx

1.12 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Fan monitoring and control
- Thermal and voltage monitoring
- Chassis intrusion detection

1.12.1 Hardware Monitoring and Fan Control

The hardware monitoring and fan control subsystem is based on the Winbond W83677HG-I device, which supports the following:

- Processor and system ambient temperature monitoring
- Chassis fan speed monitoring
- Power monitoring of +12 V, +5 V, +3.3 V, V_SM and +VCCP
- SMBus interface

1.12.2 Fan Monitoring

Fan monitoring can be implemented using Intel® Desktop Control Center or third-party software.

For information about	Refer to
The functions of the fan headers	Section 1.13.2.2, page 35

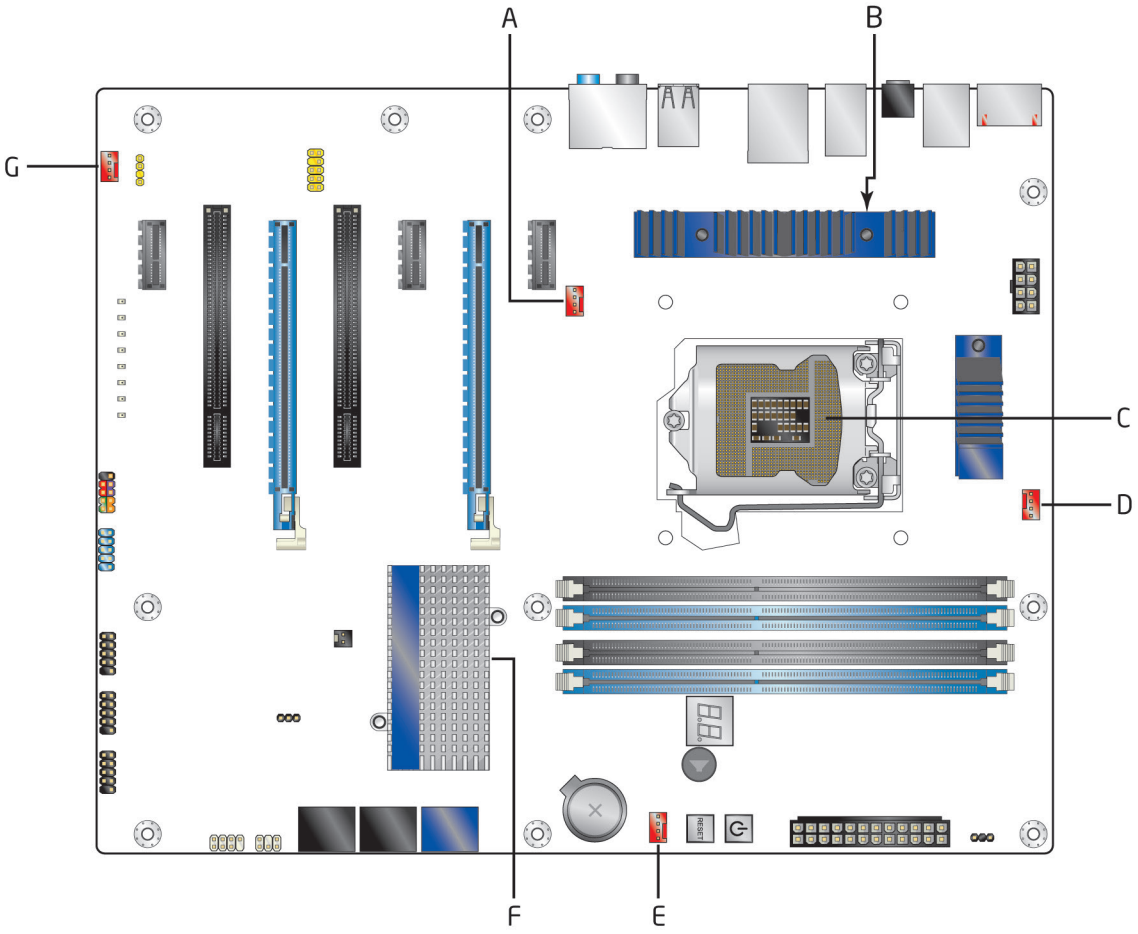
1.12.3 Chassis Intrusion and Detection

The board supports a chassis security feature that detects if the chassis cover is removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion header. When the chassis cover is removed, the mechanical switch is in the closed position.

For information about	Refer to
The location of the chassis intrusion header	Figure 11, page 45

1.12.4 Thermal Monitoring

Figure 6 shows the locations of the thermal sensors and fan headers.



Item	Description
A	Rear chassis fan header
B	Voltage regulator thermal diode
C	Thermal diode, located on processor die
D	Processor fan header
E	Front chassis fan header
F	Thermal diode, located on the Intel P67 Express Chipset
G	Auxiliary fan header

Figure 6. Thermal Sensors and Fan Headers

1.13 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan headers
  - LAN wake capabilities
  - Instantly Available PC technology
  - Wake from USB
  - Power Management Event signal (PME#) wake-up support
  - PCI Express WAKE# signal support
  - Wake from Consumer IR

1.13.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 8 on page 33)
- Support for a front panel power and sleep mode switch

Table 6 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 6. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than six seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than six seconds	Power-off (ACPI G2/G5 – Soft off)

1.13.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 7 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 7. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.13.1.2 Wake-up Devices and Events

Table 8 lists the devices or specific events that can wake the computer from specific states.

Table 8. Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S3, S4, S5 (Note 1)
RTC alarm	S3, S4, S5 (Note 1)
LAN	S3, S4, S5 (Note 1)
USB	S3
PME# signal	S3, S4, S5 (Note 1)
WAKE#	S3, S4, S5 (Note 1)
Consumer IR	S3, S4, S5 (Note 2)

Notes:

1. S4 implies operating system support only.
2. Wake from S4 and S5 is recommended by Microsoft.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.13.2 Hardware Support

CAUTION

Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

The board provides several power management hardware features, including:

- Power connector
- Fan headers
- LAN wake capabilities
- Instantly Available PC technology
- Wake from USB
- PME# signal wake-up support
- WAKE# signal wake-up support
- Wake from Consumer IR
- +5 V Standby Power Indicator LED

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line.

NOTE

The use of Wake from USB from an ACPI state requires an operating system that provides full ACPI support.

1.13.2.1 Power Connector

ATX12V-compliant power supplies can turn off the system power through system control. When an ACPI-enabled system receives the correct command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the main power connector	Figure 11, page 45
The signal names of the main power connector	Table 19, page 50

1.13.2.2 Fan Headers

The function/operation of the fan headers is as follows:

- The fans are on when the board is in the S0 state
- The fans are off when the board is off or in the S3, S4, or S5 state
- Each fan header is wired to a fan tachometer input of the hardware monitoring and fan control ASIC
- All fan headers support closed-loop fan control that can adjust the fan speed or switch the fan on or off as needed
- All fan headers have a +12 V DC connection
- 4-pin fan headers are controlled by Pulse Width Modulation

For information about	Refer to
The location of the fan headers	Figure 11, page 45
The location of the fan headers and sensors for thermal monitoring	Figure 6, page 30

1.13.2.3 LAN Wake Capabilities

CAUTION

For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the board supports LAN wake capabilities with ACPI in the following ways:

- The PCI Express WAKE# signal
- The PCI bus PME# signal for PCI 2.3 compliant LAN designs
  - By Ping
  - Magic Packet
- The onboard LAN subsystem

1.13.2.4 Instantly Available PC Technology

CAUTION

For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply.

Instantly Available PC technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 8 on page 33 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Interface Specification*. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.2 compliant add-in cards, PCI Express add-in cards, and drivers.

1.13.2.5 Wake from USB

USB bus activity wakes the computer from an ACPI S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB and is supported by the operating system.

1.13.2.6 PME# Signal Wake-up Support

When the PME# signal on the Conventional PCI bus is asserted, the computer wakes from an ACPI S3, S4, or S5 state (with Wake on PME enabled in the BIOS).

1.13.2.7 WAKE# Signal Wake-up Support

When the WAKE# signal on the PCI Express bus is asserted, the computer wakes from an ACPI S3, S4, or S5 state.

1.13.2.8 Wake from Consumer IR

CIR activity wakes the computer from an ACPI S3, S4, or S5 state.

1.13.2.9 Wake from S5

When the RTC Date and Time is set in the BIOS, the computer will automatically wake from an ACPI S5 state.

1.13.2.10 Diagnostic LEDs

The Desktop Board provides eight LEDs that allow you to monitor the board's progress through the BIOS Power-on Self-Test. At initial power on, all the LEDs are off. When the BIOS starts an activity such as memory initialization, the corresponding LED starts flashing. Once the activity has completed, the LED will remain on. Figure 7 shows the location of the diagnostic LEDs.

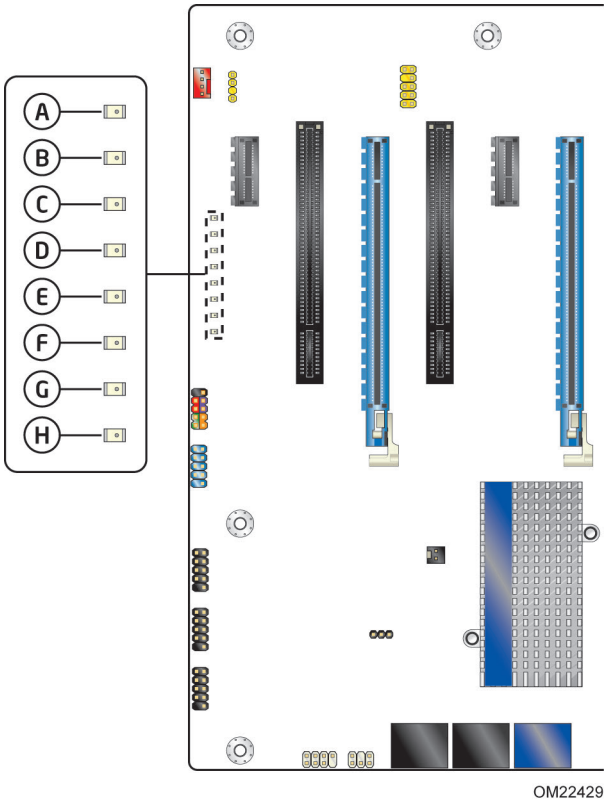


Figure 7. Location of Diagnostic LEDs

Table 9 gives a description of the LEDs shown in Figure 7.

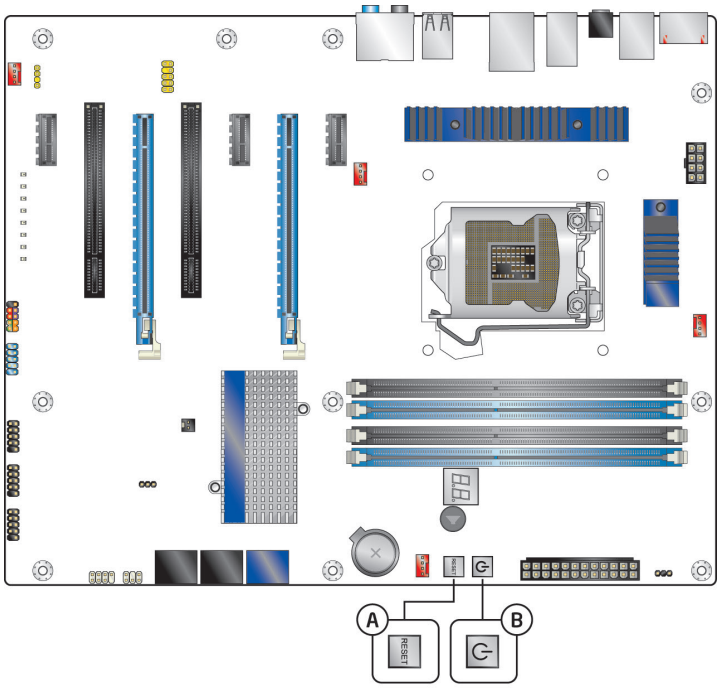
Table 9. Diagnostic LEDs

Item/Callout in Figure 7	Activity	LED Color	Description
A	Watch Dog Timer Fire/ Back to BIOS	Red	When the watch dog timer fires to reset the board, this LED will flash. In addition, this LED will light and stay on when the Back to BIOS button has been pressed.
B	Processor Initialization	Green	This LED will flash when the processor initialization activity starts. Then the LED will stay on when processor initialization is complete.
C	Memory Initialization	Green	This LED will flash when the memory initialization activity starts. Then the LED will stay on when memory initialization is complete.
D	Video Initialization	Green	This LED will flash when the video initialization activity starts. Then the LED will stay on when video initialization is complete.
E	USB Initialization	Green	This LED will flash when the USB initialization activity starts. Then the LED will stay on when USB initialization is complete.
F	Option ROM Initialization	Green	This LED will flash when the option ROM activity starts. Then the LED will stay on when option ROM initialization is complete.
G	Hard Drive Initialization	Green	This LED will flash when the hard drive activity starts. Then the LED will stay on when hard drive initialization is complete.
H	OS Start	Green	Just before BIOS transfers control to the operating system, this LED will light and stay on.

1.14 Onboard Power and Reset Buttons

The lighted onboard power button has the same behavior as the front panel power button connected via the front panel header. The onboard power button does NOT remove standby power. This button is intended for use at integration facilities for testing purposes. The power button on the front panel is recommended for all other instances of turning the computer on or off. To turn the computer off using the onboard power button, keep the button pressed down for three seconds.

The lighted onboard reset button can be used to reset the board. This button duplicates the function of the front panel reset button. Figure 8 shows the location of the onboard power and reset buttons.



Item	Description
A	Onboard reset
B	Onboard power

Figure 8. Location of the Onboard Power and Reset Buttons

CAUTION

Electrostatic discharge (ESD) can damage components. The onboard power button should be used only at an ESD workstation using an antistatic wrist strap and a conductive foam pad. If such a station is not available, some ESD protection can be provided by wearing an antistatic wrist strap and attaching it to a metal part of the computer chassis.

2 Technical Reference

2.1 Memory Resources

2.1.1 Addressable Memory

The board utilizes 32 GB of addressable system memory. Typically the address space that is allocated for Conventional PCI bus add-in cards, PCI Express configuration space, BIOS (SPI Flash device), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 32 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- BIOS/SPI Flash device (32 Mbit)
- Local APIC (19 MB)
- Direct Media Interface (40 MB)
- Front side bus interrupts (17 MB)
- PCI Express configuration space (256 MB)
- PCH base address registers PCI Express ports (up to 256 MB)
- Memory-mapped I/O that is dynamically allocated for Conventional PCI and PCI Express add-in cards (256 MB)

The board provides the capability to reclaim the physical memory overlapped by the memory mapped I/O logical address space. The board remaps physical memory from the top of usable DRAM boundary to the 4 GB boundary to an equivalent sized logical address range located just above the 4 GB boundary. Figure 9 shows a schematic of the system memory map. All installed system memory can be used when there is no overlap of system addresses.

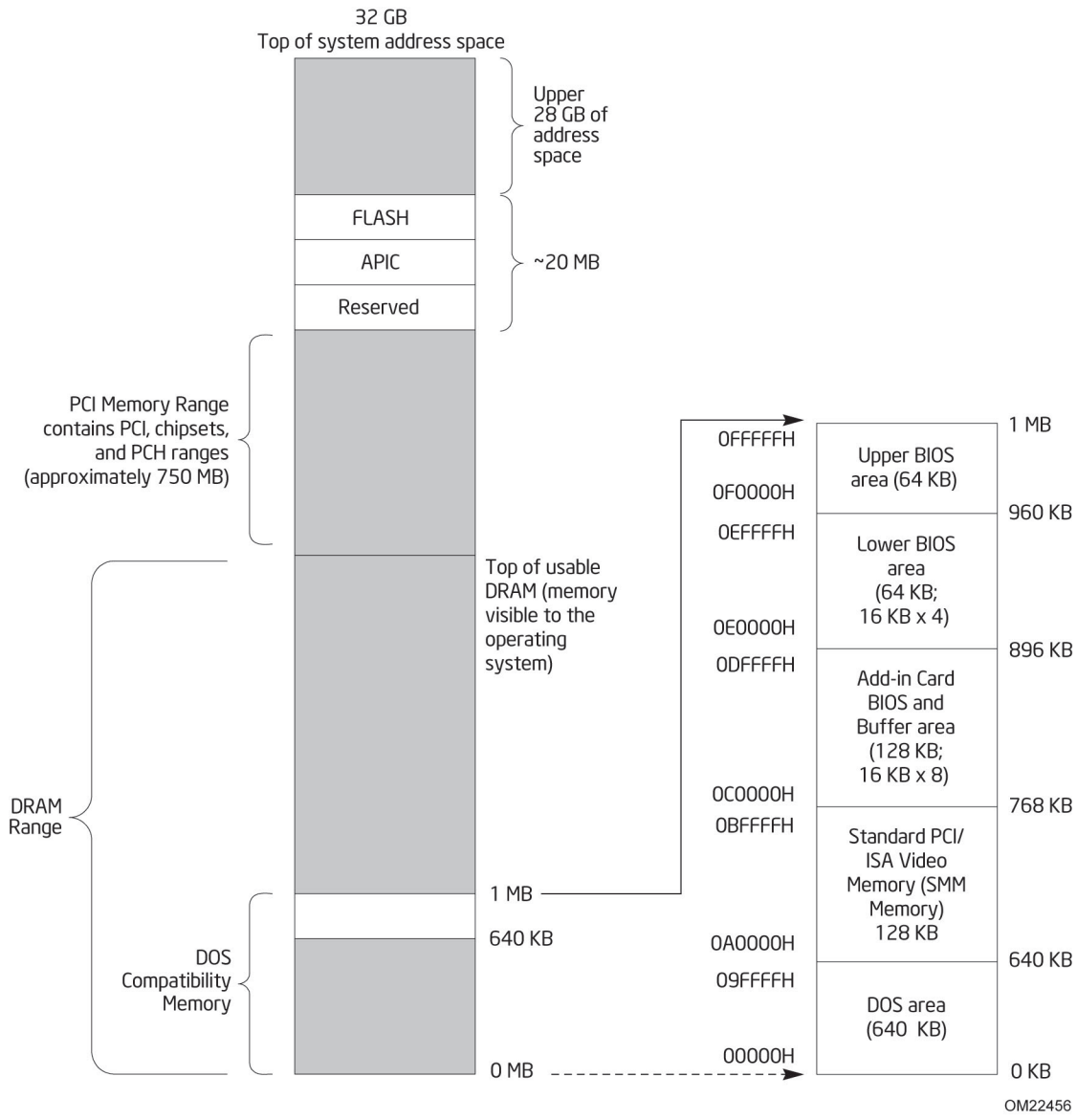


Figure 9. Detailed System Memory Address Map

2.1.2 Memory Map

Table 10 lists the system memory map.

Table 10. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 33550336 K	100000 – 7FFC00000	32764 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Potential available high DOS memory (open to the Conventional PCI bus). Dependent on video adapter used.
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.2 Connectors and Headers

CAUTION

Only the following connectors and headers have overcurrent protection: back panel and front panel USB, as well as IEEE 1394a.

The other internal connectors and headers are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors or headers to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.

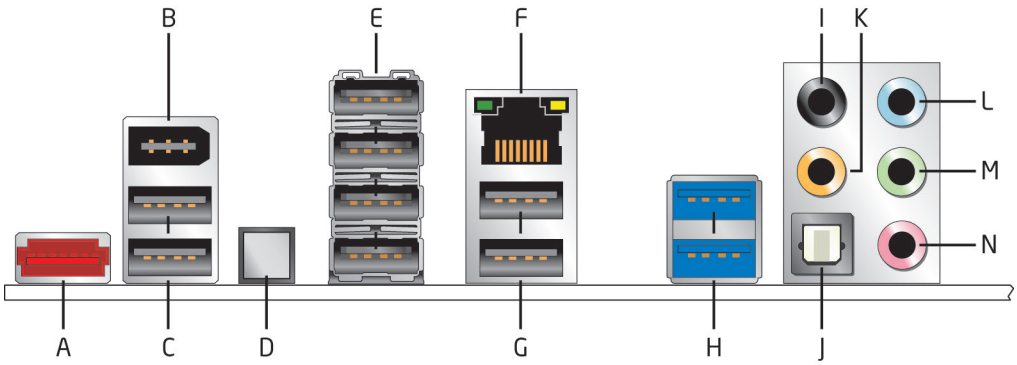
Furthermore, improper connection of USB or 1394 header single wire connectors may eventually overload the overcurrent protection and cause damage to the board.

This section describes the board's connectors. The connectors can be divided into these groups:

- Back panel I/O connectors
- Component-side I/O connectors and headers (see page 45)

2.2.1 Back Panel Connectors

Figure 10 shows the location of the back panel connectors for the board.



Item	Description
A	eSATA port
B	IEEE 1394a connector
C	USB 2.0 ports (2)
D	Back to BIOS button
E	USB 2.0 ports (4)
F	LAN
G	USB 2.0 ports (2)
H	USB 3.0 ports (2)
I	Rear surround
J	S/PDIF out (optical)
K	Center channel and LFE (subwoofer)
L	Line in
M	Line out/front speakers
N	Mic in/side surround

Figure 10. Back Panel Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

2.2.2 Component-side Connectors and Headers

Figure 11 shows the locations of the component-side connectors and headers.

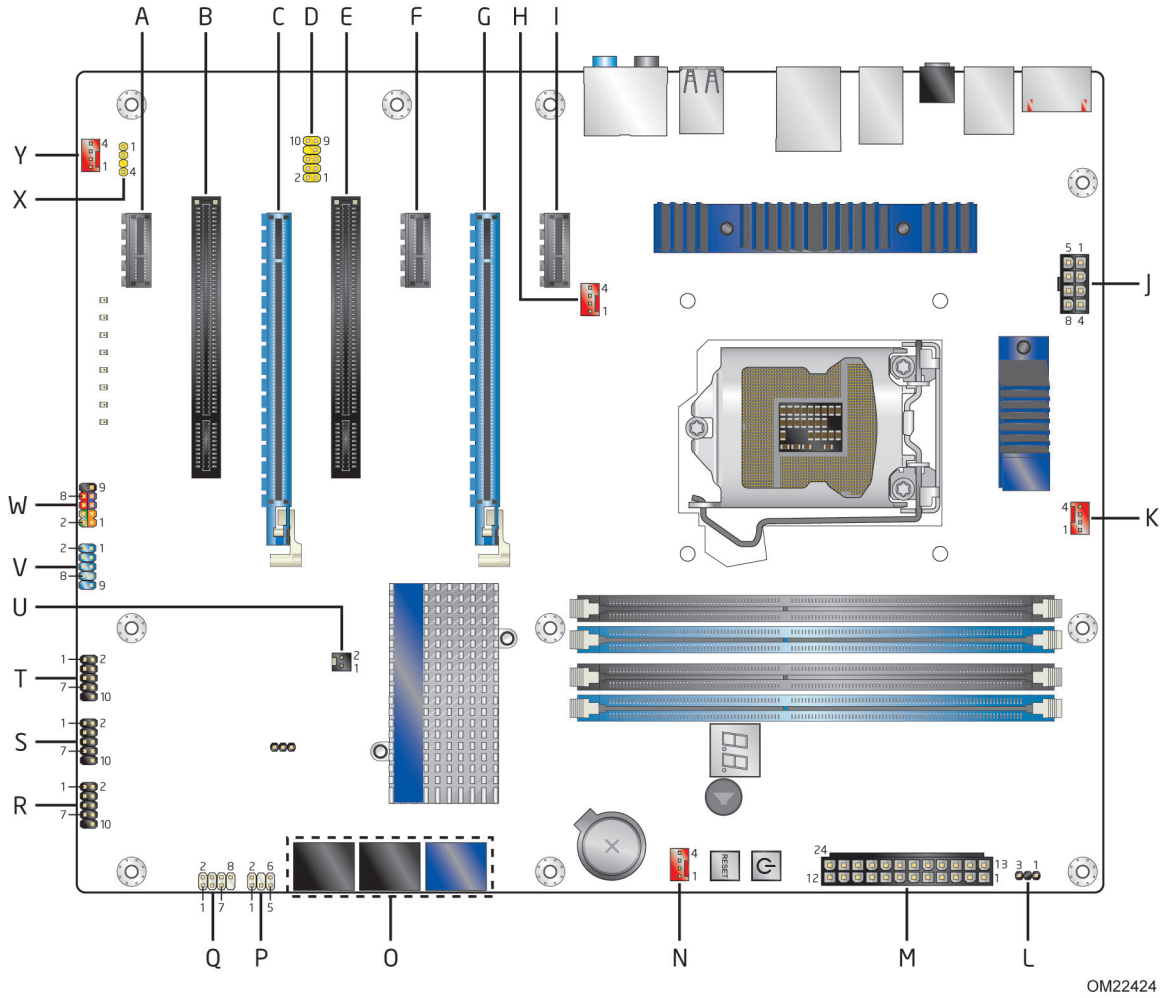


Figure 11. Component-side Connectors and Headers

Table 11 lists the component-side connectors and headers identified in Figure 11.

Table 11. Component-side Connectors and Headers Shown in Figure 11

Item/callout from Figure 11	Description
A	PCI Express x1 bus add-in card connector
B	Conventional PCI bus add-in card connector
C	PCI Express 2.0 x16 connector (x8 electrical; x16 compatible)
D	Front panel audio header
E	Conventional PCI bus add-in card connector
F	PCI Express x1 bus add-in card connector
G	PCI Express 2.0 x16 bus add-in card connector
H	Rear chassis fan header
I	PCI Express x1 bus add-in card connector
J	Processor core power connector (2 X 4)
K	Processor fan header
L	Alternate front panel LED header
M	Main power connector (2 x 12)
N	Front chassis fan header
O	SATA connectors (6)
P	Front panel CIR receiver (input) header
Q	Front panel CIR emitter (output) header
R	Front panel USB header
S	Front panel USB header
T	Front panel USB header
U	Chassis intrusion header
V	IEEE 1394a front panel header
W	Front panel header
X	S/PDIF out header
Y	Auxiliary fan header

2.2.2.1 Signal Tables for the Connectors and Headers

Table 12. IEEE 1394a Header

Pin	Signal Name	Pin	Signal Name
1	Data A (positive)	2	Data A (negative)
3	Ground	4	Ground
5	Data B (positive)	6	Data B (negative)
7	+12 V DC	8	+12 V DC
9	Key (no pin)	10	Ground

Table 13. Front Panel Audio Header

Pin	Signal Name	Pin	Signal Name
1	[Port 2] Left channel	2	Ground
3	[Port 2] Right channel	4	PRESENCE# (Dongle present)
5	[Port 1] Right channel	6	[Port 1] SENSE_RETURN
7	SENSE_SEND (Jack detection)	8	Key (no pin)
9	[Port 2] Left channel	10	[Port 2] SENSE_RETURN

Table 14. SATA Connectors

Pin	Signal Name
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7	Ground

Table 15. S/PDIF Header

Pin	Signal Name
1	Ground
2	S/PDIF out
3	Key (no pin)
4	+5 VDC

Table 16. Chassis Intrusion Header

Pin	Signal Name
1	Intruder#
2	Ground

Table 17. Processor, Front and Rear Chassis, and Auxiliary (4-Pin) Fan Headers

Pin	Signal Name
1	Ground (Note)
2	+12 V
3	FAN_TACH
4	FAN_CONTROL

Note: These fan headers use Pulse Width Modulation control for fan speed.

Table 20. Back Panel CIR Emitter (Output) Header

Pin	Signal Name
1	Emitter out 1
2	Emitter out 2
3	Ground
4	Key (no pin)
5	Jack detect 1
6	Jack detect 2

Table 21. Front Panel CIR Receiver (Input) Header

Pin	Signal Name
1	Ground
2	LED
3	NC
4	Learn-in
5	5 V standby
6	VCC
7	Key (no pin)
8	CIR Input

2.2.2.2 Add-in Card Connectors

The board has the following add-in card connectors:

- PCI Express 2.0 x16: two PCI Express 2.0 x16 connectors supporting simultaneous transfer speeds up to 8 GB/s of peak bandwidth per direction and up to 16 GB/s concurrent bandwidth.
- PCI Express 2.0 x1: three PCI Express 2.0 x1 connectors. The x1 interface supports simultaneous transfer speeds up to 1 GB/s of peak bandwidth per direction and up to 2 GB/s concurrent bandwidth.
- Conventional PCI (rev 2.3 compliant) bus: two Conventional PCI bus add-in card connectors.

Note the following considerations for the Conventional PCI bus connector:

- The Conventional PCI bus connectors are bus master capable.
- SMBus signals are routed to the Conventional PCI bus connectors. This enables Conventional PCI bus add-in boards with SMBus support to access sensor data on the desktop board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40.
  - The SMBus data line is connected to pin A41.

2.2.2.3 Power Supply Connectors

The board has the following power supply connectors:

- **Main power** – a 2 x 12 connector. This connector is compatible with 2 x 10 connectors previously used on Intel Desktop boards. The board supports the use of ATX12V power supplies with either 2 x 10 or 2 x 12 main power cables. When using a power supply with a 2 x 10 main power cable, attach that cable on the rightmost pins of the main power connector, leaving pins 11, 12, 23, and 24 unconnected.
- **Processor core power** – a 2 x 4 connector. This connector provides power directly to the processor voltage regulator and must always be used. Failure to do so will prevent the board from booting.

Table 18. Processor Core Power Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	+12 V
3	Ground	4	+12 V
5	Ground	6	+12 V
7	Ground	8	+12 V

Table 19. Main Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	13	+3.3 V
2	+3.3 V	14	-12 V
3	Ground	15	Ground
4	+5 V	16	PS-ON# (power supply remote on/off)
5	Ground	17	Ground
6	+5 V	18	Ground
7	Ground	19	Ground
8	PWRGD (Power Good)	20	No connect
9	+5 V (Standby)	21	+5 V
10	+12 V	22	+5 V
11	+12 V (Note)	23	+5 V (Note)
12	2 x 12 connector detect (Note)	24	Ground (Note)

Note: When using a 2 x 10 power supply cable, this pin will be unconnected.

For information about	Refer to
Power supply considerations	Section 2.5.1 on page 57

2.2.2.4 Front Panel Header

This section describes the functions of the front panel header. Table 20 lists the signal names of the front panel header. Figure 12 is a connection diagram for the front panel header.

Table 20. Front Panel Header

Pin	Signal	In/ Out	Description	Pin	Signal	In/ Out	Description
Hard Drive Activity LED				Power LED			
1	HD_PWR	Out	Hard disk LED pull-up to +5 V	2	HDR_BLNK_GRN	Out	Front panel green LED
3	HDA#	Out	Hard disk active LED	4	HDR_BLNK_YEL	Out	Front panel yellow LED
Reset Switch				On/Off Switch			
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
Power				Not Connected			
9	+5 V		Power	10	N/C		Not connected

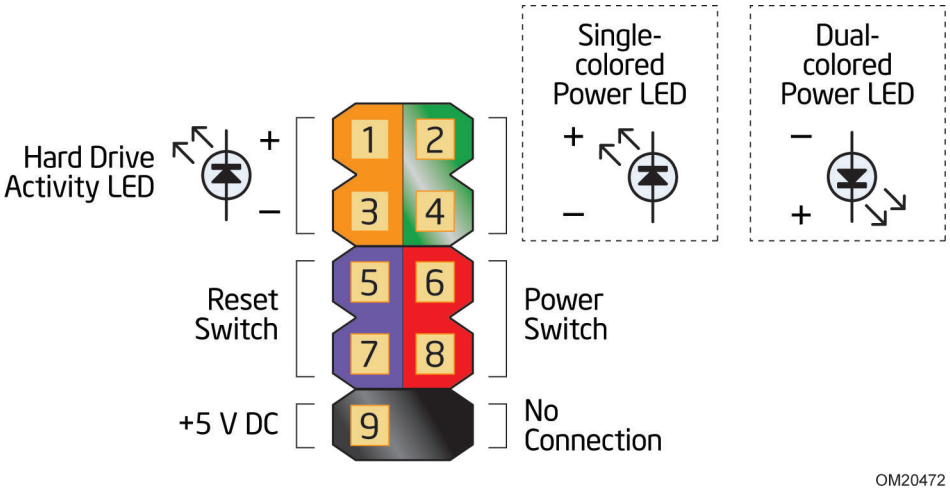


Figure 12. Connection Diagram for Front Panel Header

2.2.2.4.1 Hard Drive Activity LED Header

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires a SATA hard drive or optical drive connected to an onboard SATA connector.

2.2.2.4.2 Reset Switch Header

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

2.2.2.4.3 Power/Sleep LED Header

Pins 2 and 4 can be connected to a one- or two-color LED. Table 21 shows the possible states for a one-color LED. Table 22 shows the possible states for a two-color LED.

Table 21. States for a One-Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running

Table 22. States for a Two-Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Steady Yellow	Sleeping

NOTE

The colors listed in Table 21 and Table 22 are suggested colors only. Actual LED colors are chassis-specific.

2.2.2.4.4 Power Switch Header

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.2.2.5 Front Panel USB Headers

Figure 13 is a connection diagram for the front panel USB headers.

NOTE

- *The +5 V DC power on the USB headers is fused.*
- *Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.*

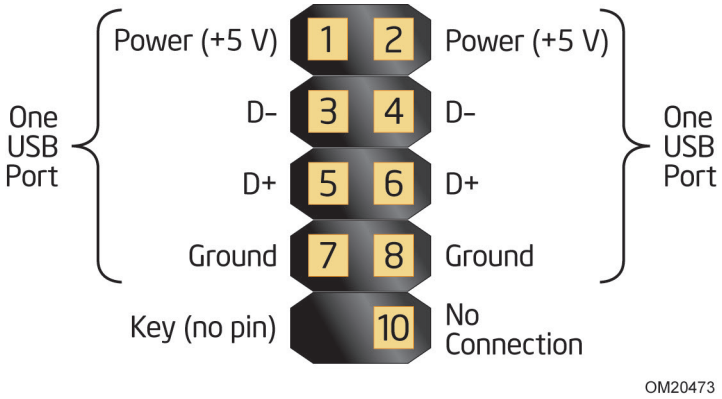


Figure 13. Connection Diagram for Front Panel USB Headers

2.3 Jumper Block

CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 14 shows the location of the jumper block. The 3-pin jumper block determines the BIOS Setup program's mode. Table 23 describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configure mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

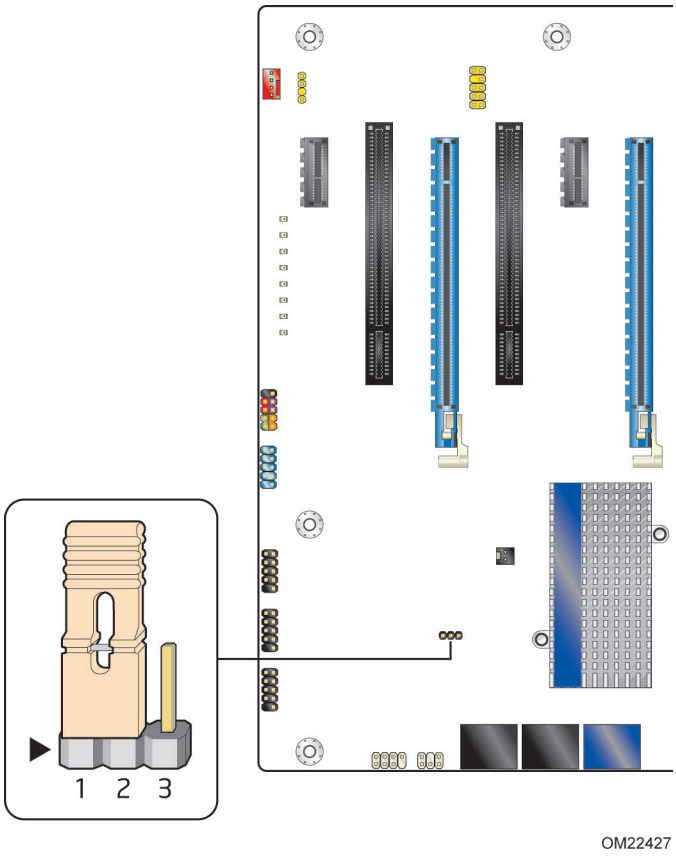


Figure 14. Location of the Jumper Block

Table 23. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting	Configuration
Normal	1-2	The BIOS uses current configuration information and passwords for booting.
Configure	2-3	After the POST runs, Setup runs automatically. The maintenance menu is displayed. Note that this Configure mode is the only way to clear the BIOS/CMOS settings. Press F9 (restore defaults) while in Configure mode to restore the BIOS/CMOS settings to their default values.
Recovery	None	The BIOS attempts to recover the BIOS configuration. A recovery CD or flash drive is required.

2.4 Mechanical Considerations

2.4.1 Form Factor

The board is designed to fit into an ATX-form-factor chassis. Figure 15 illustrates the mechanical form factor for the board. Dimensions are given in inches [millimeters]. The outer dimensions are 12.00 inches by 9.60 inches [304.80 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification.

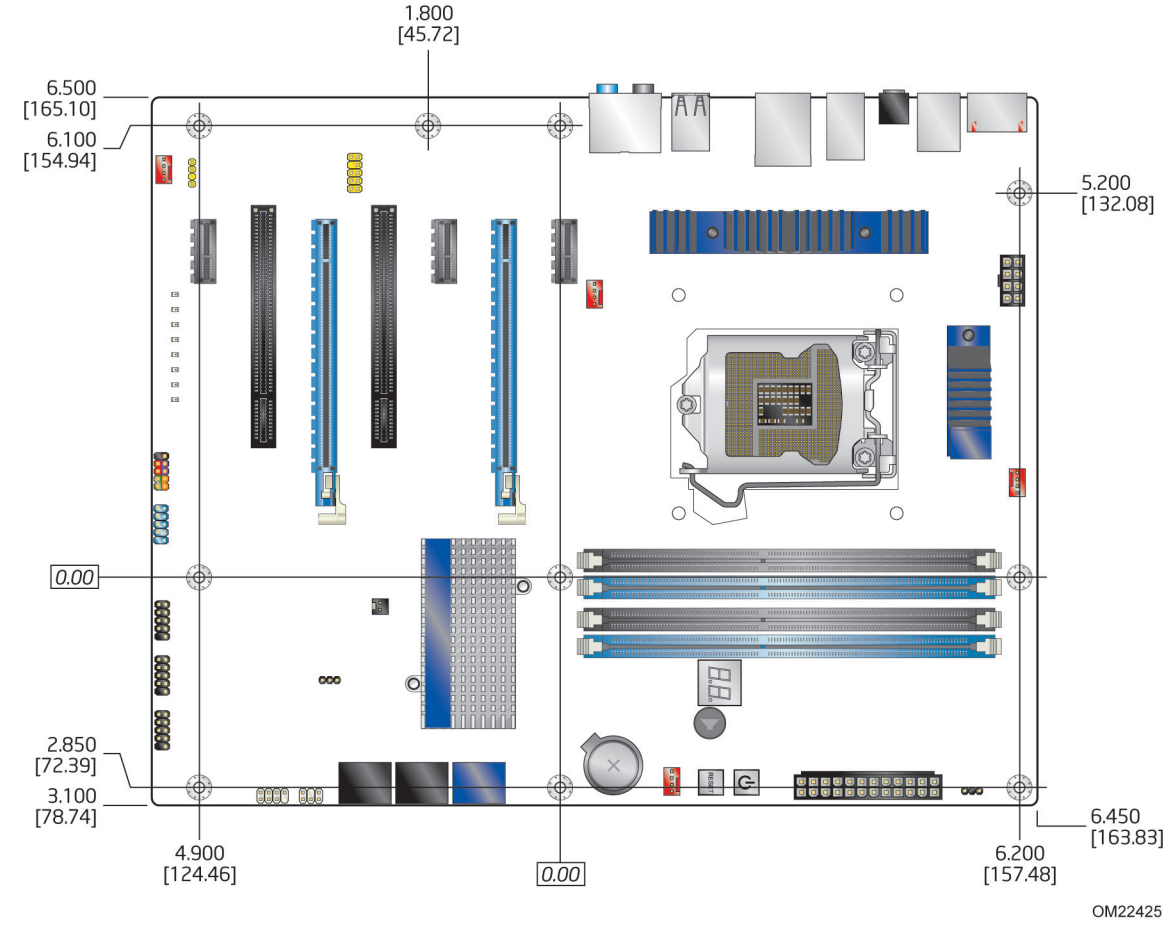


Figure 15. Board Dimensions

2.5 Electrical Considerations

2.5.1 Power Supply Considerations

CAUTION

The +5 V standby line from the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the indicated parameters of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails
- The current capability of the +5 VSB line
- All timing parameters
- All voltage tolerances

For example, for a system consisting of a supported 95 W processor (see Section 1.4 on page 16 for a list of supported processors), 4 GB DDR3 RAM, one high end video card, one hard disk drive, one optical drive, and all board peripherals enabled, the minimum recommended power supply is 460 W. Table 24 lists the recommended power supply current values.

Table 24. Recommended Power Supply Current Values

Output Voltage	3.3 V	5 V	12 V1	12 V2	-12 V	5 VSB
Current	22 A	20 A	16 A	16 A	0.3 A	1.5 A

For information about	**Refer to**
Selecting an appropriate power supply	http://support.intel.com/support/motherboards/desktop/sb/CS-026472.htm

2.5.2 Fan Header Current Capability

CAUTION

The processor fan must be connected to the processor fan header, not to a chassis fan header. Connecting the processor fan to a chassis fan header may result in onboard component damage that will halt fan operation.

Table 25 lists the current capability of the fan headers.

Table 25. Fan Header Current Capability

Fan Header	Maximum Available Current
Processor fan	1.5 A
Front chassis fan	1.5 A
Rear chassis fan	1.5 A
Auxiliary chassis fan	1.5 A

2.5.3 Add-in Board Considerations

The board is designed to provide 2 A (average) of current for each add-in board from the +5 V rail. The total +5 V current draw for add-in boards for a fully loaded board (all six expansion slots filled) must not exceed the system's power supply +5 V maximum current or 14 A in total.

2.6 Thermal Considerations

CAUTION

*A chassis with a maximum internal ambient temperature of 38 °C at the processor fan inlet is a requirement. Use a processor heat sink that provides **omni-directional** airflow to maintain required airflow across the processor voltage regulator area. If a non omni-directional thermal solution is used customer might need to provide supplemental cooling to the processor voltage regulator area.*

CAUTION

Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the board. For a list of chassis that have been tested with Intel desktop boards please refer to the following website:

http://www3.intel.com/cd/channel/reseller/asmo-na/eng/tech_reference/53211.htm

All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.

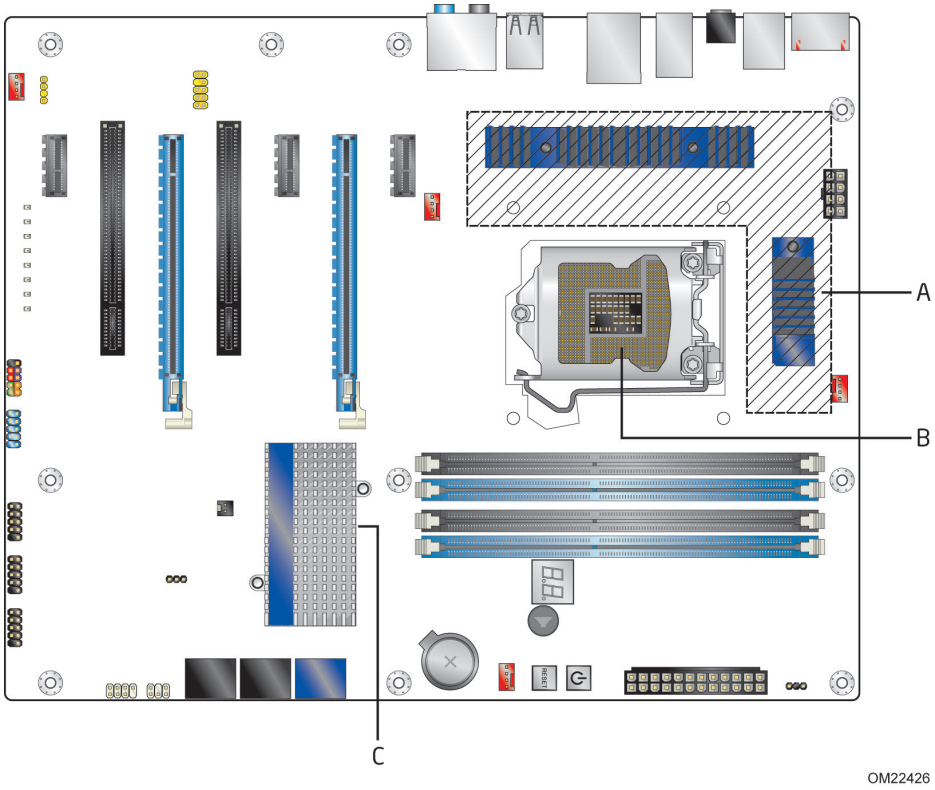
CAUTION

Ensure that the ambient temperature does not exceed the board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.8.

CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (shown in Figure 16) can reach a temperature of up to 85 °C in an open chassis.

Figure 16 shows the locations of the localized high temperature zones.



Item	Description
A	Processor voltage regulator area
B	Processor
C	Intel P67 Express Chipset

Figure 16. Localized High Temperature Zones

Table 26 provides maximum case temperatures for the components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the board.

Table 26. Thermal Considerations for Components

Component	Maximum Case Temperature
Processor	For processor case temperature, see processor datasheets and processor specification updates
Intel P67 Express Chipset	104 °C (under bias)

For information about	Refer to
Processor datasheets and specification updates	Section 1.3, page 16

2.7 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Telcordia SR-332, Method I Case 1 50% electrical stress, 55 ºC ambient. The MTBF prediction is used to estimate repair rates and spare parts requirements. The MTBF data is calculated from predicted data at 55 ºC. The MTBF for the board is 219,854.08 hours.

2.8 Environmental

Table 27 lists the environmental specifications for the board.

Table 27. Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-20 °C to +70 °C (Note)		
Operating	0 °C to +55 °C The operating temperature of the board may be determined by measuring the air temperature from within 1 inch of the edge of the chipset/PCH heatsink and 1 inch above the board, in a closed chassis, while the system is in operation.		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/second²		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec²)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz: 0.02 g² Hz (flat)		
Packaged	5 Hz to 40 Hz: 0.015 g² Hz (flat)		
	40 Hz to 500 Hz: 0.015 g² Hz sloping down to 0.00015 g² Hz		

Note: Before attempting to operate this board, the overall temperature of the board must be above the minimum operating temperature specified. It is recommended that the board temperature be at least room temperature before attempting to power on the board.

3 Overview of BIOS Features

3.1 Introduction

The board uses an Intel BIOS that is stored in the Serial Peripheral Interface Flash Memory (SPI Flash) and can be updated using a disk-based program. The SPI Flash contains the BIOS Setup program, POST, the PCI auto-configuration utility, LAN EEPROM information, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as BGP6710J.86A.

When the BIOS Setup configuration jumper is set to configure mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Configuration	Performance	Security	Power	Boot	Exit

NOTE

The maintenance menu is displayed only when the board is in configure mode. Section 2.3 on page 54 shows how to put the board in configure mode.

Table 28 lists the BIOS Setup program menu features.

Table 28. BIOS Setup Program Menu Bar

Maintenance	Main	Configura-tion	Performance	Security	Power	Boot	Exit
Clears passwords and displays processor information	Displays processor and memory configuration	Configures advanced features available through the chipset	Configures Memory, Bus and Processor overrides	Sets passwords and security features	Configures power management features and power supply controls	Selects boot options	Saves or discards changes to Setup program options

Table 29 lists the function keys available for menu screens.

Table 29. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

3.2 BIOS Flash Memory Organization

The Serial Peripheral Interface Flash Memory (SPI Flash) includes a 32 Mbit (4096 KB) flash memory device.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information. Additional board information can be found in the BIOS under the Additional Information header under the Main BIOS page.

3.5 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.
7. Additional USB legacy feature options can be access by using Intel Integrator Toolkit.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB hard drive), an optical drive, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires booting from DOS. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB hard drive), or an optical drive.
- Intel® F7 switch allows a user to select where the BIOS .bio file is located and perform the update from that location/device. Similar to performing a BIOS Recovery without removing the BIOS configuration jumper.

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
BIOS update utilities	http://support.intel.com/support/motherboards/desktop/sb/CS-022312.htm.

3.6.1 Language Support

The BIOS Setup program and help messages are supported in US English. Check the Intel web site for support.

3.6.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be augmented with a custom splash screen. The Intel Integrator's Toolkit that is available from Intel can be used to create a custom splash screen.

NOTE

If you add a custom splash screen, it will share space with the Intel branded logo.

For information about	Refer to
Intel® Integrator Toolkit	http://developer.intel.com/design/motherbd/software/itk/
Additional Intel® software tools	http://developer.intel.com/products/motherboard/DP67BG/tools.htm and http://developer.intel.com/design/motherbd/software.htm

3.7 BIOS Recovery

It is unlikely that anything will interrupt a BIOS update; however, if an interruption occurs, the BIOS could be damaged. Table 30 lists the drives and media types that can and cannot be used for BIOS recovery. The BIOS recovery media does not need to be made bootable.

Table 30. Acceptable Drives/Media Types for BIOS Recovery

Media Type	Can be used for BIOS recovery?
Optical drive connected to the SATA interface	Yes
USB removable drive (a USB Flash Drive, for example)	Yes
USB diskette drive (with a 1.44 MB diskette)	No
USB hard disk drive	No

For information about	Refer to
BIOS recovery	http://www.intel.com/support/motherboards/desktop/sb/cs-023360.htm

3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drive, USB drive, USB flash drive, optical drive, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the optical drive third. If enabled, the last default boot device is the network.

3.8.1 Optical Drive Boot

Booting from the optical drive is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, the optical drive is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the optical drive, the system will attempt to boot from the next defined drive.

3.8.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

3.8.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.8.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices (as set in the BIOS setup program's Boot Device Priority Submenu). Table 31 lists the boot device menu options.

Table 31. Boot Device Menu Options

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, saves changes, and boots from the selected device
<Esc>	Exits the menu without saving changes

3.9 Adjusting Boot Speed

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Optimized BIOS boot parameters
- Enabling the new Hyperboot feature

3.9.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as "power-up to data ready" in less than eight seconds to minimize hard drive startup delays.
- Select an optical drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

3.9.2 BIOS Boot Optimizations

Use of the following BIOS Setup program settings reduces the POST execution time.

- In the Boot Menu, set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.
- The BIOS will automatically not load the option ROM for the SATA controller if no drives are installed in it during POST.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from zero to 30 seconds by 5 second increments (using the Hard Disk Pre-Delay feature of the Advanced Menu in the Drive Configuration Submenu of the BIOS Setup program).

3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.

Table 32 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 32. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

3.11 BIOS Performance Features

The BIOS includes the following options to provide custom performance enhancements when using an Intel Core i7, Intel Core i5, and Intel Core i3 processors in an LGA 1155 socket.

- Processor frequency adjustment
- Processor voltage adjustment
- Memory clock adjustments
- Memory voltage adjustments
- QPI Bus voltage adjustment
- PCI Bus speed adjustment

4 Error Messages and Beep Codes

4.1 Speaker

The board-mounted speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker	Figure 1, page 13

4.2 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS causes the board's speaker to beep an error message describing the problem (see Table 33).

Table 33. BIOS Beep Codes

Type	Pattern	Frequency
F2 Setup/F10 Boot Menu Prompt	One 0.5 second beep when BIOS is ready to accept keyboard input	932 Hz
BIOS update in progress	None	
Video error	On-off (1.0 second each) two times, then 2.5-second pause (off), entire pattern repeats (beeps and pause) once and the BIOS will continue to boot.	932 Hz When no VGA option ROM is found.
Memory error	On-off (1.0 second each) three times, then 2.5-second pause (off), entire pattern repeats (beeps and pause) until the system is powered off.	932 Hz
Thermal trip warning	Alternate high and low beeps (1.0 second each) for 8 beeps, followed by system shut down.	High beep 2000 Hz Low beep 1500 Hz

4.3 Front-panel Power LED Blink Codes

Whenever a recoverable error occurs during POST, the BIOS causes the board's front panel power LED to blink an error message describing the problem (see Table 34).

Table 34. Front-panel Power LED Blink Codes

Type	Pattern	Note
F2 Setup/F10 Boot Menu Prompt	None	
BIOS update in progress	Off when the update begins, then on for 0.5 seconds, then off for 0.5 seconds. The pattern repeats until the BIOS update is complete.	
Video error	On-off (1.0 second each) two times, then 2.5-second pause (off), entire pattern repeats (blink and pause) until the system is powered off.	When no VGA option ROM is found.
Memory error	On-off (1.0 second each) three times, then 2.5-second pause (off), entire pattern repeats (blinks and pause) until the system is powered off.	
Thermal trip warning	Each beep will be accompanied by the following blink pattern: .25 seconds on, .25 seconds off, .25 seconds on, .25 seconds off. This will result in a total of 16 blinks.	

4.4 BIOS Error Messages

Table 35 lists the error messages and provides a brief description of each.

Table 35. BIOS Error Messages

Error Message	Explanation
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed, then memory may be bad.
No Boot Device Available	System did not find a device to boot.

4.5 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

NOTE

The POST card must be installed in PCI bus connector 1.

The following tables provide information about the POST codes generated by the BIOS:

- Table 36 lists the Port 80h POST code ranges
- Table 37 lists the Port 80h POST codes themselves
- Table 38 lists the Port 80h POST sequence

NOTE

In the tables listed above, all POST codes and range values are listed in hexadecimal.

Table 36. Port 80h POST Code Ranges

Range	Subsystem
0x00 – 0x05	Entering SX states S0 to S5.
0x10, 0x20, 0x30, 0x40, 0x50	Resuming from SX states. 0x10 –0x20 – S2, 0x30 – S3, etc.
0x08 – 0x0F	Security (SEC) phase
0x11 0x1F	PEI phase pre MRC execution
0x21 – 0x29	MRC memory detection
0x2A – 0x2F	PEI phase post MRC execution
0x31 – 0x35	Recovery
0x36 – 0x3F	Platform DXE driver
0x41 – 0x4F	CPU Initialization (PEI, DXE, SMM)
0x50 – 0x5F	I/O Buses: PCI, USB, ATA etc. 0x5F is an unrecoverable error. Start with PCI.
0x60 – 0x6F	BDS
0x70 – 0x7F	Output devices: All output consoles.
0x80 – 0x8F	For future use
0x90 – 0x9F	Input devices: Keyboard/Mouse.
0xA0 – 0xAF	For future use
0xB0 – 0xBF	Boot Devices: Includes fixed media and removable media. Not that critical since consoles should be up at this point.
0xC0 – 0xCF	For future use
0xD0 – 0xDF	For future use
0xF0 – 0xFF	

Table 37. Port 80h POST Codes

Port 80 Code	Progress Code Enumeration
	ACPI S States
0x00,0x01,0x02,0x03,0x04,0x05	Entering S0, S2, S3, S4, or S5 state
0x10,0x20,0x30,0x40,0x50	Resuming from S2, S3, S4, S5
	Security Phase (SEC)
0x08	Starting BIOS execution after CPU BIST
0x09	SPI prefetching and caching
0x0A	Load BSP microcode
0x0B	Load APs microcodes
0x0C	Platform program baseaddresses
0x0D	Wake Up All APs
0x0E	Initialize NEM
0x0F	Pass entry point of the PEI core
	PEI before MRC
	PEI Platform driver
0x11	Set bootmode, GPIO init
0x12	Early chipset register programming including graphics init
0x13	Basic PCH init, discrete device init (1394, SATA)
0x14	LAN init
0x15	Exit early platform init driver
	PEI SMBUS
0x16	SMBUSriver init
0x17	Entry to SMBUS execute read/write
0x18	Exit SMBUS execute read/write
	PEI CK505 Clock Programming
0x19	Entry to CK505 programming
0x1A	Exit CK505 programming
	PEI Over-Clock Programming
0x1B	Entry to entry to PEI over-clock programming
0x1C	Exit PEI over-clock programming
	Memory
0x21	MRC entry point
0x23	Reading SPD from memory DIMMs
0x24	Detecting presence of memory DIMMs
0x27	Configuring memory
0x28	Testing memory
0x29	Exit MRC driver
	PEI after MRC
0x2A	Start to Program MTRR Settings
0x2B	Done Programming MTRR Settings

continued

Table 37. Port 80h POST Codes (continued)

Port 80 Code	Progress Code Enumeration
	PEIMs/Recovery
0x31	Crisis Recovery has initiated
0x33	Loading recovery capsule
0x34	Start recovery capsule/ valid capsule is found
	CPU Initialization
	CPU PEI Phase
0x41	Begin CPU PEI Init
0x42	XMM instruction enabling
0x43	End CPU PEI Init
	CPU PEI SMM Phase
0x44	Begin CPU SMM Init smm relocate bases
0x45	Smm relocate bases for APs
0x46	End CPU SMM Init
	CPU DXE Phase
0x47	CPU DXE Phase begin
0x48	Refresh memory space attributes according to MTRRs
0x49	Load the microcode if needed
0x4A	Initialize strings to HII database
0x4B	Initialize MP support
0x4C	CPU DXE Phase End
	CPU DXE SMM Phase
0x4D	CPU DXE SMM Phase begin
0x4E	Relocate SM bases for all APs
0x4F	CPU DXE SMM Phase end
	I/O BUSES
0x50	Enumerating PCI buses
0x51	Allocating resources to PCI bus
0x52	Hot Plug PCI controller initialization
	USB
0x58	Resetting USB bus
0x59	Reserved for USB
	ATA/ATAPI/SATA
0x5A	Resetting PATA/SATA bus and all devices
0x5B	Reserved for ATA

continued

Table 37. Port 80h POST Codes (continued)

Port 80 Code	Progress Code Enumeration
	BDS
0x60	BDS driver entry point initialize
0x61	BDS service routine entry point (can be called multiple times)
0x62	BDS Step2
0x63	BDS Step3
0x64	BDS Step4
0x65	BDS Step5
0x66	BDS Step6
0x67	BDS Step7
0x68	BDS Step8
0x69	BDS Step9
0x6A	BDS Step10
0x6B	BDS Step11
0x6C	BDS Step12
0x6D	BDS Step13
0x6E	BDS Step14
0x6F	BDS return to DXE core (should not get here)
	Keyboard (PS/2 or USB)
0x90	Resetting keyboard
0x91	Disabling the keyboard
0x92	Detecting the presence of the keyboard
0x93	Enabling the keyboard
0x94	Clearing keyboard input buffer
0x95	Instructing keyboard controller to run Self Test (PS/2 only)
	Mouse (PS/2 or USB)
0x98	Resetting mouse
0x99	Detecting mouse
0x9A	Detecting presence of mouse
0x9B	Enabling mouse
	Fixed Media
0xB0	Resetting fixed media
0xB1	Disabling fixed media
0xB2	Detecting presence of a fixed media (IDE hard drive detection etc.)
0xB3	Enabling/configuring a fixed media

continued

Table 37. Port 80h POST Codes (continued)

Port 80 Code	Progress Code Enumeration
	Removable Media
0xB8	Resetting removable media
0xB9	Disabling removable media
0xBA	Detecting presence of a removable media (IDE, CDROM detection etc.)
0xBB	Enabling/configuring a removable media
	DXE Core
0xE4	Entered DXE phase
	BDS
0xE7	Waiting for user input
0xE8	Checking password
0xE9	Entering BIOS setup
0xEB	Calling Legacy Option ROMs
	Runtime Phase/EFI OS Boot
0xF8	EFI boot service ExitBootServices ( ) has been called
0xF9	EFI runtime service SetVirtualAddressMap ( ) has been called

Table 38. Typical Port 80h POST Sequence

POST Code	Description
21	Initializing a chipset component
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
25	Configuring memory
28	Testing memory
34	Loading recovery capsule
E4	Entered DXE phase
12	Starting application processor initialization
13	SMM initialization
50	Enumerating PCI buses
51	Allocating resourced to PCI bus
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
95	Keyboard Self Test
EB	Calling Video BIOS
58	Resetting USB bus
5A	Resetting PATA/SATA bus and all devices
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
5A	Resetting PATA/SATA bus and all devices
28	Testing memory
90	Resetting keyboard
94	Clearing keyboard input buffer
E7	Waiting for user input
01	INT 19
00	Ready to boot

5 Regulatory Compliance and Battery Disposal Information

5.1 Regulatory Compliance

This section contains the following regulatory compliance information for Intel Desktop Board DP67BG:

- Safety standards
- European Union Declaration of Conformity statement
- Product Ecology statements
- Electromagnetic Compatibility (EMC) standards
- Product certification markings

5.1.1 Safety Standards

Intel Desktop Board DP67BG complies with the safety standards stated in Table 39 when correctly installed in a compatible host system.

Table 39. Safety Standards

Standard	Title
CSA/UL 60950-1	Information Technology Equipment – Safety - Part 1: General Requirements (USA and Canada)
EN 60950-1	Information Technology Equipment – Safety - Part 1: General Requirements (European Union)
IEC 60950-1	Information Technology Equipment – Safety - Part 1: General Requirements (International)

5.1.2 European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the product Intel® Desktop Board DP67BG is in conformity with all applicable essential requirements necessary for CE marking, following the provisions of the European Council Directive 2004/108/EC (EMC Directive), 2006/95/EC (Low Voltage Directive), and 2002/95/EC (ROHS Directive).

The product is properly CE marked demonstrating this conformity and is for distribution within all member states of the EU with no restrictions.

This product follows the provisions of the European Directives 2004/108/EC, 2006/95/EC, and 2002/95/EC.

Čeština Tento výrobek odpovídá požadavkům evropských směrnic 2004/108/EC, 2006/95/EC a 2002/95/EC.

Dansk Dette produkt er i overensstemmelse med det europæiske direktiv 2004/108/EC, 2006/95/EC & 2002/95/EC.

Dutch Dit product is in navolging van de bepalingen van Europees Directief 2004/108/EC, 2006/95/EC & 2002/95/EC.

Eesti Antud toode vastab Euroopa direktiivides 2004/108/EC, ja 2006/95/EC ja 2002/95/EC kehtestatud nõuetele.

Suomi Tämä tuote noudattaa EU-direktiivin 2004/108/EC, 2006/95/EC & 2002/95/EC määräyksiä.

Français Ce produit est conforme aux exigences de la Directive Européenne 2004/108/EC, 2006/95/EC & 2002/95/EC.

Deutsch Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2004/108/EC, 2006/95/EC & 2002/95/EC.

Ελληνικά Το παρόν προϊόν ακολουθεί τις διατάξεις των Ευρωπαϊκών Οδηγιών 2004/108/EC, 2006/95/EC και 2002/95/EC.

Magyar E termék megfelel a 2004/108/EC, 2006/95/EC és 2002/95/EC Európai Irányelv előírásainak.

Icelandic Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2004/108/EC, 2006/95/EC, & 2002/95/EC.

Italiano Questo prodotto è conforme alla Direttiva Europea 2004/108/EC, 2006/95/EC & 2002/95/EC.

Latviešu Šis produkts atbilst Eiropas Direktīvu 2004/108/EC, 2006/95/EC un 2002/95/EC noteikumiem.

Lietuvių Šis produktas atitinka Europos direktyvų 2004/108/EC, 2006/95/EC, ir 2002/95/EC nuostatas.

Malti Dan il-prodott hu konformi mal-provvedimenti tad-Direttivi Ewropej 2004/108/EC, 2006/95/EC u 2002/95/EC.

Norsk Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 2004/108/EC, 2006/95/EC & 2002/95/EC.

Polski Niniejszy produkt jest zgodny z postanowieniami Dyrektyw Unii Europejskiej 2004/108/EC, 206/95/EC i 2002/95/EC.

Portuguese Este produto cumpre com as normas da Diretiva Européia 2004/108/EC, 2006/95/EC & 2002/95/EC.

Español Este producto cumple con las normas del Directivo Europeo 2004/108/EC, 2006/95/EC & 2002/95/EC.

Slovensky Tento produkt je v súlade s ustanoveniami európskych direktív 2004/108/EC, 2006/95/EC a 2002/95/EC.

Slovenščina Izdelek je skladen z določbami evropskih direktiv 2004/108/EC, 2006/95/EC in 2002/95/EC.

Svenska Denna produkt har tillverkats i enlighet med EG-direktiv 2004/108/EC, 2006/95/EC & 2002/95/EC.

Türkçe Bu ürün, Avrupa Birliği'nin 2004/108/EC, 2006/95/EC ve 2002/95/EC yönergelerine uyar.

5.1.3 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

5.1.3.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

5.1.3.2 Recycling Considerations

As part of its commitment to environmental responsibility, Intel has implemented the Intel Product Recycling Program to allow retail consumers of Intel's branded products to return used products to selected locations for proper recycling.

Please consult the http://www.intel.com/intel/other/ehs/product_ecology for the details of this program, including the scope of covered products, available locations, shipping instructions, terms and conditions, etc.

中文

作为其对环境责任之承诺的部分，英特尔已实施 Intel Product Recycling Program（英特尔产品回收计划），以允许英特尔品牌产品的零售消费者将使用过的产品退还至指定地点作恰当的重复使用处理。

请参考http://www.intel.com/intel/other/ehs/product_ecology 了解此计划的详情，包括涉及产品之范围、回收地点、运送指导、条款和条件等。

Deutsch

Als Teil von Intels Engagement für den Umweltschutz hat das Unternehmen das Intel Produkt-Recyclingprogramm implementiert, das Einzelhandelskunden von Intel Markenprodukten ermöglicht, gebrauchte Produkte an ausgewählte Standorte für ordnungsgemäßes Recycling zurückzugeben.

Details zu diesem Programm, einschließlich der darin eingeschlossenen Produkte, verfügbaren Standorte, Versandanweisungen, Bedingungen usw., finden Sie auf der http://www.intel.com/intel/other/ehs/product_ecology

Español

Como parte de su compromiso de responsabilidad medioambiental, Intel ha implantado el programa de reciclaje de productos Intel, que permite que los consumidores al detalle de los productos Intel devuelvan los productos usados en los lugares seleccionados para su correspondiente reciclado.

Consulte la http://www.intel.com/intel/other/ehs/product_ecology para ver los detalles del programa, que incluye los productos que abarca, los lugares disponibles, instrucciones de envío, términos y condiciones, etc.

Français

Dans le cadre de son engagement pour la protection de l'environnement, Intel a mis en œuvre le programme Intel Product Recycling Program (Programme de recyclage des produits Intel) pour permettre aux consommateurs de produits Intel de recycler les produits usés en les retournant à des adresses spécifiées.

Visitez la page Web http://www.intel.com/intel/other/ehs/product_ecology pour en savoir plus sur ce programme, à savoir les produits concernés, les adresses disponibles, les instructions d'expédition, les conditions générales, etc.

日本語

インテルでは、環境保護活動の一環として、使い終えたインテル
ブランド製品を指定の場所へ返送していただき、リサイクルを適切に行えるよう、インテル製品リサイクル
プログラムを発足させました。

対象製品、返送先、返送方法、ご利用規約など、このプログラムの詳細情報は、http://www.intel.com/intel/other/ehs/product_ecology（英語）をご覧ください。

Malay

Sebagai sebahagian daripada komitmennya terhadap tanggungjawab persekitaran, Intel telah melaksanakan Program Kitar Semula Produk untuk membenarkan pengguna-pengguna runcit produk jenama Intel memulangkan produk terguna ke lokasi-lokasi terpilih untuk dikitarkan semula dengan betul.

Sila rujuk http://www.intel.com/intel/other/ehs/product_ecology untuk mendapatkan butir-butir program ini, termasuklah skop produk yang dirangkumi, lokasi-lokasi tersedia, arahan penghantaran, terma & syarat, dsb.

Portuguese

Como parte deste compromisso com o respeito ao ambiente, a Intel implementou o Programa de Reciclagem de Produtos para que os consumidores finais possam enviar produtos Intel usados para locais selecionados, onde esses produtos são reciclados de maneira adequada.

Consulte o site http://www.intel.com/intel/other/ehs/product_ecology (em Inglês) para obter os detalhes sobre este programa, inclusive o escopo dos produtos cobertos, os locais disponíveis, as instruções de envio, os termos e condições, etc.

Russian

В качестве части своих обязательств к окружающей среде, в Intel создана программа утилизации продукции Intel (Product Recycling Program) для предоставления конечным пользователям марок продукции Intel возможности возврата используемой продукции в специализированные пункты для должной утилизации.

Пожалуйста, обратитесь на веб-сайт http://www.intel.com/intel/other/ehs/product_ecology за информацией об этой программе, принимаемых продуктах, местах приема, инструкциях об отправке, положениях и условиях и т.д.

Türkçe

Intel, çevre sorumluluğuna bağımlılığının bir parçası olarak, perakende tüketicilerin Intel markalı kullanılmış ürünlerini belirlenmiş merkezlere iade edip uygun şekilde geri dönüştürmesini amaçlayan Intel Ürünleri Geri Dönüşüm Programı'nı uygulamaya koymuştur.

Bu programın ürün kapsamı, ürün iade merkezleri, nakliye talimatları, kayıtlar ve şartlar v.s dahil bütün ayrıntılarını ögrenmek için lütfen http://www.intel.com/intel/other/ehs/product_ecology

Web sayfasına gidin.

5.1.4 EMC Regulations

Intel Desktop Board DP67BG complies with the EMC regulations stated in Table 40 when correctly installed in a compatible host system.

Table 40. EMC Regulations

Regulation	Title
FCC 47 CFR Part 15, Subpart B	Title 47 of the Code of Federal Regulations, Part 15, Subpart B, Radio Frequency Devices. (USA)
ICES-003	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
EN55022	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurement. (International)
VCCI V-3, V-4	Voluntary Control for Interference by Information Technology Equipment. (Japan)
KN-22, KN-24	Korean Communications Commission – Framework Act on Telecommunications and Radio Waves Act (South Korea)
CNS 13438	Bureau of Standards, Metrology, and Inspection (Taiwan)

FCC Declaration of Conformity

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation, 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications to the equipment not expressly approved by Intel Corporation could void the user's authority to operate the equipment.

Tested to comply with FCC standards for home or office use.

Canadian Department of Communications Compliance Statement

This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le présent appareil numerique német pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la classe B prescrites dans le Réglement sur le broullage radioélectrique édicté par le ministére des Communications du Canada.

Japan VCCI Statement

Japan VCCI Statement translation: This is a Class B product based on the standard of the Voluntary Control Council for Interference from Information Technology Equipment (VCCI). If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＢ情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
取扱説明書に従って正しい取り扱いをして下さい。

Korea Class B Statement

Korea Class B Statement translation: This equipment is for home use, and has acquired electromagnetic conformity registration, so it can be used not only in residential areas, but also other areas.

이 기기는 가정용(B급)으로 전자파적합등록을 한 기기로서 주로 가정에서 사용하는 것을 목적 으로 하며, 모든 지역에서 사용할 수 있습니다.

5.1.5 ENERGY STAR* 5.0, e-Standby, and ErP Compliance

The US Department of Energy and the US Environmental Protection Agency have continually revised the ENERGY STAR requirements. Intel has worked directly with these two governmental agencies in the definition of new requirements.

Intel Desktop Board DP67BG meets the following program requirements in an adequate system configuration, including appropriate selection of an efficient power supply:

- Energy Star v5.0, category B
- EPEAT*
- Korea e-Standby
- European Union Energy-related Products Directive 2009 (ErP) Lot 6

For information about	Refer to
ENERGY STAR requirements and recommended configurations	http://www.intel.com/go/energystar
Electronic Product Environmental Assessment Tool (EPEAT)	http://www.epeat.net/
Korea e-Standby Program	http://www.kemco.or.kr/new_eng/pg02/pg02100300.asp
European Union Energy-related Products Directive 2009 (ErP)	http://ec.europa.eu/enterprise/policies/sustainable-business/sustainable-product-policy/ecodesign/index_en.htm

5.1.6 Regulatory Compliance Marks (Board Level)

Intel Desktop Board DP67BG has the regulatory compliance marks shown in Table 41.

Table 41. Regulatory Compliance Marks

Description	Mark
UL joint US/Canada Recognized Component mark. Includes adjacent UL file number for Intel Desktop Boards: E210882.	
FCC Declaration of Conformity logo mark for Class B equipment.	
CE mark. Declaring compliance to the European Union (EU) EMC directive, Low Voltage directive, and RoHS directive.	
Australian Communications Authority (ACA) and New Zealand Radio Spectrum Management (NZ RSM) C-tick mark. Includes adjacent Intel supplier code number, N-232.	
Japan VCCI (Voluntary Control Council for Interference) mark.	
Korea Certification mark. Includes an adjacent KCC (Korean Communications Commission) certification number: KCC-REM-CPU-DP67BG	
Taiwan BSMI (Bureau of Standards, Metrology and Inspections) mark. Includes adjacent Intel company number, D33025.	
Printed wiring board manufacturer's recognition mark. Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side).	V-0
China RoHS/Environmentally Friendly Use Period Logo: This is an example of the symbol used on Intel Desktop Boards and associated collateral. The color of the mark may vary depending upon the application. The Environmental Friendly Usage Period (EFUP) for Intel Desktop Boards has been determined to be 10 years.	

5.2 Battery Disposal Information

CAUTION

Risk of explosion if the battery is replaced with an incorrect type. Batteries should be recycled where possible. Disposal of used batteries must be in accordance with local environmental regulations.

PRÉCAUTION

Risque d'explosion si la pile usagée est remplacée par une pile de type incorrect. Les piles usagées doivent être recyclées dans la mesure du possible. La mise au rebut des piles usagées doit respecter les réglementations locales en vigueur en matière de protection de l'environnement.

FORHOLDSREGEL

Eksplosionsfare, hvis batteriet erstattes med et batteri af en forkert type. Batterier bør om muligt genbruges. Bortskaffelse af brugte batterier bør foregå i overensstemmelse med gældende miljølovgivning.

OBS!

Det kan oppstå eksplosjonsfare hvis batteriet skiftes ut med feil type. Brukte batterier bør kastes i henhold til gjeldende miljølovgivning.

VIKTIGT!

Risk för explosion om batteriet ersätts med felaktig batterityp. Batterier ska kasseras enligt de lokala miljövårdsbestämmelserna.

VARO

Räjähdysvaara, jos pariston tyyppi on väärä. Paristot on kierrätettävä, jos se on mahdollista. Käytetyt paristot on hävitettävä paikallisten ympäristömääräysten mukaisesti.

VORSICHT

Bei falschem Einsetzen einer neuen Batterie besteht Explosionsgefahr. Die Batterie darf nur durch denselben oder einen entsprechenden, vom Hersteller empfohlenen Batterietyp ersetzt werden. Entsorgen Sie verbrauchte Batterien den Anweisungen des Herstellers entsprechend.

AVVERTIMENTO

Esiste il pericolo di un esplosione se la pila non viene sostituita in modo corretto. Utilizzare solo pile uguali o di tipo equivalente a quelle consigliate dal produttore. Per disfarsi delle pile usate, seguire le istruzioni del produttore.

PRECAUCIÓN

Existe peligro de explosión si la pila no se cambia de forma adecuada. Utilice solamente pilas iguales o del mismo tipo que las recomendadas por el fabricante del equipo. Para deshacerse de las pilas usadas, siga igualmente las instrucciones del fabricante.

WAARSCHUWING

Er bestaat ontploffingsgevaar als de batterij wordt vervangen door een onjuist type batterij. Batterijen moeten zoveel mogelijk worden gerecycled. Houd u bij het weggooien van gebruikte batterijen aan de plaatselijke milieuwetgeving.

ATENÇÃO

Haverá risco de explosão se a bateria for substituída por um tipo de bateria incorreto. As baterias devem ser recicladas nos locais apropriados. A eliminação de baterias usadas deve ser feita de acordo com as regulamentações ambientais da região.

AŚCIAROŽZNAŚĆ

Існуе рызыка выбуху, калі заменены акумулятар неправільнага тыпу. Акумулятары павінны, па магчымасці, перепрацоўвацца. Пазбаўляцца ад старых акумулятараў патрэбна згодна з мясцовым заканадаўствам па экалогіі.

UPOZORNÌNÍ

V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.

Προσοχή

Υπάρχει κίνδυνος για έκρηξη σε περίπτωση που η μπαταρία αντικατασταθεί από μία λανθασμένου τύπου. Οι μπαταρίες θα πρέπει να ανακυκλώνονται όταν κάτι τέτοιο είναι δυνατό. Η απόρριψη των χρησιμοποιημένων μπαταριών πρέπει να γίνεται σύμφωνα με τους κατά τόπο περιβαλλοντικούς κανονισμούς.

VIGYÁZAT

Ha a telepet nem a megfelelő típusú telepre cseréli, az felrobbanhat. A telepeket lehetőség szerint újra kell hasznosítani. A használt telepeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.

注意

異なる種類の電池を使用すると、爆発の危険があります。リサイクルが可能な地域であれば、電池をリサイクルしてください。使用後の電池を廃棄する際には、地域の環境規制に従ってください。

AWAS

Risiko letupan wujud jika bateri digantikan dengan jenis yang tidak betul. Bateri sepatutnya dikitar semula jika boleh. Pelupusan bateri terpakai mestilah mematuhi peraturan alam sekitar tempatan.

OSTRZEŻENIE

Istnieje niebezpieczeństwo wybuchu w przypadku zastosowania niewłaściwego typu baterii. Zużyte baterie należy w miarę możliwości utylizować zgodnie z odpowiednimi przepisami ochrony środowiska.

PRECAUŢIE

Risc de explozie, dacă bateria este înlocuită cu un tip de baterie necorespunzător. Bateriile trebuie reciclate, dacă este posibil. Depozitarea bateriilor uzate trebuie să respecte reglementările locale privind protecţia mediului.

ВНИМАНИЕ

При использовании батареи несоответствующего типа существует риск ее взрыва. Батареи должны быть утилизированы по возможности. Утилизация батарей должна проводится по правилам, соответствующим местным требованиям.

UPOZORNENIE

Ak batériu vymeníte za nesprávny typ, hrozí nebezpečenstvo jej výbuchu.
Batérie by sa mali podľa možnosti vždy recyklovať. Likvidácia použitých batérií sa musí vykonávať v súlade s miestnymi predpismi na ochranu životného prostredia.

POZOR

Zamenjava baterije z baterijo drugačnega tipa lahko povzroči eksplozijo.
Če je mogoče, baterije reciklirajte. Rabljene baterije zavrzite v skladu z lokalnimi okoljevarstvenimi predpisi.

คำเตือน

ระวังการระเบิดที่เกิดจากเปลี่ยนแบตเตอรี่ผิดประเภท หากเป็นไปได้ ควรนำแบตเตอรี่ไปรีไซเคิล การทิ้งแบตเตอรี่ใช้แล้วต้องเป็นไปตามกฎข้อบังคับด้านสิ่งแวดล้อมของท้องถิ่น.

UYARI

Yanlış türde pil takıldığında patlama riski vardır. Piller mümkün olduğunda geri dönüştürülmelidir. Kullanılmış piller, yerel çevre yasalarına uygun olarak atılmalıdır.

ОСТОРОГА

Використовуйте батареї правильного типу, інакше існуватиме ризик вибуху. Якщо можливо, використані батареї слід утилізувати. Утилізація використаних батарей має бути виконана згідно місцевих норм, що регулюють охорону довкілля.

UPOZORNĚNÍ

V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.

ETTEVAATUST

Kui patarei asendatakse uue ebasobivat tüüpi patareiga, võib tekkida plahvatusoht. Tühjad patareid tuleb võimaluse korral viia vastavasse kogumispunkti. Tühjade patareide äraviskamisel tuleb järgida kohalikke keskkonnakaitse alaseid reegleid.

FIGYELMEZTETÉS

Ha az elemet nem a megfelelő típusúra cseréli, felrobbanhat. Az elemeket lehetőség szerint újra kell hasznosítani. A használt elemeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.

UZMANĪBU

Pastāv eksplozijas risks, ja baterijas tiek nomainītas ar nepareiza veida baterijām. Ja iespējams, baterijas vajadzētu nodot attiecīgos pieņemšanas punktos. Bateriju izmešanai atkritumos jānotiek saskaņā ar vietējiem vides aizsardzības noteikumiem.

DĖMESIO

Naudojant netinkamo tipo baterijas įrenginys gali sprogti. Kai tik įmanoma, baterijas reikia naudoti pakartotinai. Panaudotas baterijas išmesti būtina pagal vietinius aplinkos apsaugos nuostatus.

ATTENZJONI

Riskju ta' splużjoni jekk il-batterija tinbidel b'tip ta' batterija mhux korrett. Il-batteriji għandhom jiġu riċiklati fejn hu possibbli. Ir-rimi ta' batteriji użati għandu jsir skond ir-regolamenti ambjentali lokali.

OSTRZEŻENIE

Ryzyko wybuchu w przypadku wymiany na baterie niewłaściwego typu. W miarę możliwości baterie należy poddać recyklingowi. Zużytych baterii należy pozbywać się zgodnie z lokalnie obowiązującymi przepisami w zakresie ochrony środowiska.